Intel® Desktop Boards D915GAV/D915GAG

Technical Product Specification

June 2004

Order Number: C68600-001

The Intel® Desktop Board D915GAV/D915GAG may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D915GAV/D915GAG Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D915GAV/D915GAG Technical Product Specification.	June 2004

This product specification applies to only standard Intel® Desktop Boards D915GAV and D915GAV with BIOS identifier EV91510A.86A.

Changes to this specification will be published in the Intel Desktop Board D915GAV/D915GAG Specification Update before being incorporated into a revision of this document.

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Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for these Intel® Desktop Boards: D915GAV and D915GAG. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Boards D915GAV and D915GAG and their components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Desktop Boards D915GAV and D915GAG
2	A map of the resources of the Desktop Boards
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

INTEGRATOR'S NOTES

Integrator's notes are used to call attention to information that may be useful to system integrators.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Boards D915GAV and D915GAG, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

1 Product Description

1.1 PCI Bus Terminology Change 11
1.2 Board Differences 11
1.3 Overview 12
1.3.1 Feature Summary 12
1.3.2 Manufacturing Options 13
1.3.3 Board Layouts 14
1.3.4 Block Diagram 18
1.4 Online Support 19
1.5 Processor 19
1.6 System Memory 20
1.6.1 Memory Configurations 22
1.7 Intel® 915G Chipset 26
1.7.1 Intel 915G Graphics Subsystem 26
1.7.2 USB 28
1.7.3 IDE Support 28
1.7.4 Real-Time Clock, CMOS SRAM, and Battery 30
1.8 PCI Express Connectors 30
1.9 I/O Controller 30
1.9.1 Serial Ports 31
1.9.2 Parallel Port 31
1.9.3 Diskette Drive Controller 31
1.9.4 Keyboard and Mouse Interface 31
1.10 Audio Subsystem 32
1.10.1 Audio Subsystem Software 32
1.10.2 Audio Connectors 32
1.10.3 Intel® High Definition Audio Subsystem 33
1.11 LAN Subsystem 34
1.11.1 Intel® 82562EZ Physical Layer Interface Device 34
1.11.2 RJ-45 LAN Connector with Integrated LEDs 34
1.11.3 Alert Standard Format (ASF) Support 35
1.11.4 LAN Subsystem Software 35
1.11.5 Intel® Wireless Connect Technology (Optional) 35
1.12 Hardware Management Subsystem 36
1.12.1 Hardware Monitoring and Fan Control ASIC 36
1.12.2 Thermal Monitoring 37
1.12.3 Fan Monitoring 39
1.12.4 Chassis Intrusion and Detection 39
1.13 Power Management 40
1.13.1 ACPI 40
1.13.2 Hardware Support 42

1.14 Trusted Platform Module (Optional) 46
1.14.1 System Requirements 46
1.14.2 Warning of Potential Data Loss 46
1.14.3 Security Precautions 47
1.14.4 Trusted Platform Module Ownership 48
1.14.5 Enabling the Trusted Platform Module 48
1.14.6 Assuming Trusted Platform Module Ownership 49
1.14.7 Recovery Procedures 50
1.14.8 Clearing Trusted Platform Module Ownership 51
1.14.9 Software Support 51

2 Technical Reference

2.1 Introduction 53
2.2 Memory Resources 53
2.2.1 Addressable Memory 53
2.2.2 Memory Map 55
2.3 DMA Channels 55
2.4 Fixed I/O Map 56
2.5 PCI Configuration Space Map 57
2.6 Interrupts 58
2.7 PCI Conventional Interrupt Routing Map 59
2.8 Connectors 61
2.8.1 Back Panel Connectors 62
2.8.2 Component-side Connectors 64
2.9 Jumper Block 75
2.10 Mechanical Considerations 76
2.10.1 D915GAV Board Form Factor 76
2.10.2 D915GAG Board Form Factor 77
2.10.3 I/O Shield 78
2.11 Electrical Considerations 79
2.11.1 DC Loading 79
2.11.2 Add-in Board Considerations 79
2.11.3 Fan Connector Current Capability 80
2.11.4 Power Supply Considerations 80
2.12 Thermal Considerations 81
2.13 Reliability 83
2.14 Environmental 84
2.15 Regulatory Compliance 85
2.15.1 Safety Regulations 85
2.15.2 EMC Regulations 85
2.15.3 European Union Declaration of Conformity Statement 86
2.15.4 Product Ecology Statements 87
2.15.5 Product Certification Markings (Board Level) 88

3 Overview of BIOS Features

3.1 Introduction 89
3.2 BIOS Flash Memory Organization 90
3.3 Resource Configuration 90
3.3.1 PCI Autoconfiguration 90
3.3.2 PCI IDE Support 90
3.4 System Management BIOS (SMBIOS) 91
3.5 Legacy USB Support 91
3.6 BIOS Updates 92
3.6.1 Language Support 92
3.6.2 Custom Splash Screen 92
3.7 Boot Options 93
3.7.1 CD-ROM Boot 93
3.7.2 Network Boot 93
3.7.3 Booting Without Attached Devices 93
3.7.4 Changing the Default Boot Device During POST 93
3.8 Fast Booting Systems with Intel® Rapid BIOS Boot 94
3.8.1 Peripheral Selection and Configuration 94
3.8.2 Intel Rapid BIOS Boot 94
3.9 BIOS Security Features 95

4 Error Messages and Beep Codes

4.1 BIOS Error Messages 97
4.2 Port 80h POST Codes 99
4.3 Bus Initialization Checkpoints 103
4.4 Speaker 104
4.5 BIOS Beep Codes 104

Figures

1. D915GAV Board Components 14
2. D915GAG Board Components 16
3. Block Diagram 18
4. Memory Channel and DIMM Configuration 22
5. Dual Channel (Interleaved) Mode Configuration with Two DIMMs 23
6. Dual Channel (Interleaved) Mode Configuration with Three DIMMs 23
7. Dual Channel (Interleaved) Mode Configuration with Four DIMMs 24
8. Single Channel (Asymmetric) Mode Configuration with One DIMM 25
9. Single Channel (Asymmetric) Mode Configuration with Three DIMMs 25
10. Front/Back Panel Audio Connector Options for High Definition Audio Subsystem 33
11. High Definition Audio Subsystem Block Diagram 33
12. LAN Connector LED Locations 34
13. Thermal Monitoring for D915GAV Board 37
14. Thermal Monitoring for D915GAG Board 38
15. Location of the Standby Power Indicator LED 45
16. Detailed System Memory Address Map 54
17. Back Panel Connectors 62
18. D915GAV Board Component-side Connectors 64
19. D915GAG Board Component-side Connectors 66

20. Connection Diagram for Front Panel Connector 72
21. Connection Diagram for Front Panel USB Connectors 74
22. Connection Diagram for IEEE 1394a Connectors 74
23. Location of the Jumper Block 75
24. D915GAV Board Dimensions 76
25. D915GAG Board Dimensions 77
26. I/O Shield Dimensions 78
27. Processor Heatsink for Omni-directional Airflow 81
28. Localized High Temperature Zones 82

Tables

1. Summary of Board Differences 11
2. Feature Summary 12
3. Manufacturing Options 13
4. D915GAV Board Components Shown in Figure 1. 15
5. D915GAG Board Components Shown in Figure 2. 17
6. Supported System Bus Frequency and Memory Speed Combinations 20
7. Supported Memory Configurations 21
8. LAN Connector LED States 34
9. Effects of Pressing the Power Switch 40
10. Power States and Targeted System Power 41
11. Wake-up Devices and Events 42
12. System Memory Map 55
13. DMA Channels 55
14. I/O Map 56
15. PCI Configuration Space Map 57
16. Interrupts 58
17. PCI Interrupt Routing Map 60
18. Back Panel Connectors Shown in Figure 17. 63
19. Component-side Connectors Shown in Figure 18. 65
20. Component-side Connectors Shown in Figure 19. 67
21. S/PDIF Connector (Optional) 68
22. ATAPI CD-ROM Connector (Optional) 68
23. Front Panel Audio Connector 68
24. Serial Port B Connector (optional) 68
25. Chassis Intrusion Connector 68
26. SCSI Hard Drive Activity LED Connector (Optional) 69
27. Serial ATA Connectors 69
28. Processor Fan Connector 69
29. Chassis Fan Connectors 69
30. Main Power Connector 70
31. ATX12V Power Connector 71
32. Alternate Power Connector 71
33. Auxiliary Front Panel Power/Sleep LED Connector 72
34. Front Panel Connector 72
35. States for a One-Color Power LED 73
36. States for a Two-Color Power LED 73
37. BIOS Setup Configuration Jumper Settings 75

38. DC Loading Characteristics 79
39. Fan Connector Current Capability 80
40. Thermal Considerations for Components 83
41. Environmental Specifications 84
42. Safety Regulations 85
43. EMC Regulations 85
44. Product Certification Markings 88
45. BIOS Setup Program Menu Bar 90
46. BIOS Setup Program Function Keys 90
47. Boot Device Menu Options 93
48. Supervisor and User Password Functions 95
49. BIOS Error Messages 97
50. Uncompressed INIT Code Checkpoints 99
51. Boot Block Recovery Code Checkpoints 99
52. Runtime Code Uncompressed in F000 Shadow RAM 100
53. Bus Initialization Checkpoints 103
54. Upper Nibble High Byte Functions 103
55. Lower Nibble High Byte Functions 104
56. Beep Codes 104

1 Product Description

What This Chapter Contains

1.1 PCI Bus Terminology Change 11
1.2 Board Differences 11
1.3 Overview 12
1.4 Online Support 19
1.5 Processor 19
1.6 System Memory 20
1.7 Intel® 915G Chipset 26
1.8 PCI Express Connectors 30
1.9 I/O Controller 30
1.10 Audio Subsystem 32
1.11 LAN Subsystem 34
1.12 Hardware Management Subsystem 36
1.13 Power Management 40
1.14 Trusted Platform Module (Optional) 46

1.1 PCI Bus Terminology Change

Previous generations of Intel® Desktop Boards used an add-in card connector referred to as PCI. This generation of Intel Desktop Boards adds a new technology for add-in cards: PCI Express. The 32-bit parallel bus previously referred to as PCI is now called PCI Conventional.

1.2 Board Differences

This TPS describes these Intel Desktop Boards: D915GAV and D915GAG. The Desktop Boards are identical with the exception of the items listed in Table 1.

Table 1. Summary of Board Differences

D915GAV	• ATX Form Factor • Four PCI Conventional bus connectors • Two PCI Express x1 bus add-in card connectors • Three chassis fan connectors (front chassis, rear chassis 1, and rear chassis 2)
D915GAG	• microATX Form Factor • Two PCI Conventional bus connectors • One PCI Express* x1 bus add-in card connector • Two chassis fan connectors (front chassis and rear chassis)

NOTE

Most of the illustrations in this document show only the Desktop Board D915GAV. When there are significant differences between the two Desktop Boards, illustrations of both boards are provided.

1.3 Overview

1.3.1 Feature Summary

Table 2 summarizes the major features of the Desktop Boards D915GAV and D915GAG.

Table 2. Feature Summary

Form Factor	• D915GAV: ATX (12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters]) • D915GAG: microATX Form Factor (9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters])
Processor	Support for an Intel® Pentium® 4 processor in an LGA775 socket with an 800 or 533 MHz system bus
Memory	• Four DDR SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR 400 MHz and DDR 333 MHz DIMMs • Support for up to 4 GB of system memory
Chipset	Intel® 915G Chipset, consisting of: • Intel® 82915G Graphics Memory Controller Hub (GMCH) • Intel® 82801FB I/O Controller Hub (ICH6) • 4 Mbit Firmware Hub (FWH)
Video	Intel® GMA900 onboard graphics subsystem
Audio	Intel® High Definition Audio subsystem using the Realtek* ALC860 audio codec
I/O Control	LPC Bus I/O controller
USB	Support for USB 2.0 devices
Peripheral Interfaces	• Eight USB ports • One serial port • One parallel port • Four Serial ATA interfaces • One Parallel ATA IDE interface with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports
LAN Support	10/100 Mbits/sec LAN subsystem using the Intel® 82562EZ Platform LAN Connect (PLC) device
BIOS	• Intel/AMI BIOS (resident in the 4 Mbit FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Support for PCI Express Revision 1.0a • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports

continued

Table 2. Feature Summary (continued)

Expansion Capabilities	• PCI Conventional bus connectors (four on the D915GAV; two on the D915GAG) • PCI Express x1 bus add-in card connectors (two on the D915GAV; one on the D915GAG) • One PCI Express x16 bus add-in card connector (both boards)
Hardware Monitor Subsystem	• Hardware monitoring and fan control ASIC • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Three fan connectors • Three fan sense inputs used to monitor fan activity • Fan speed control

1.3.2 Manufacturing Options

Table 3 describes the manufacturing options on the Desktop Boards D915GAV and D915GAG. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 3. Manufacturing Options

ATAPI CD-ROM Connector	A connector for attaching an internal CD-ROM drive to the onboard audio subsystem
ATX fan connector	Additional fan connector for use in larger chassis (D915GAV board only)
IEEE-1394a Interface	IEEE-1394a controller and three IEEE-1394a connectors (one back panel connector, two front-panel connectors)
Intel® 82801FBW I/O Controller Hub (ICH6W)	I/O controller Hub that supports Intel® Wireless Connect Technology
SCSI Hard Drive Activity LED Connector	Allows add-in hard drive controllers (SCSI or other) to use the same LED as the onboard IDE controller.
Serial Port B	Second serial port accessible via a connector on the component side of the board
S/PDIF Connector	A 1 x 3 connector (mounted on the component side of the board) that provides digital audio signals in S/PDIF format
Trusted Platform Module (TPM)	A component that enhances platform security

For information about	Refer to
Available configurations for the Desktop Boards D915GAV and D915GAG	Section 1.4, page 19

1.3.3 Board Layouts

Figure 1 shows the location of the major components on the Desktop Board D915GAV.

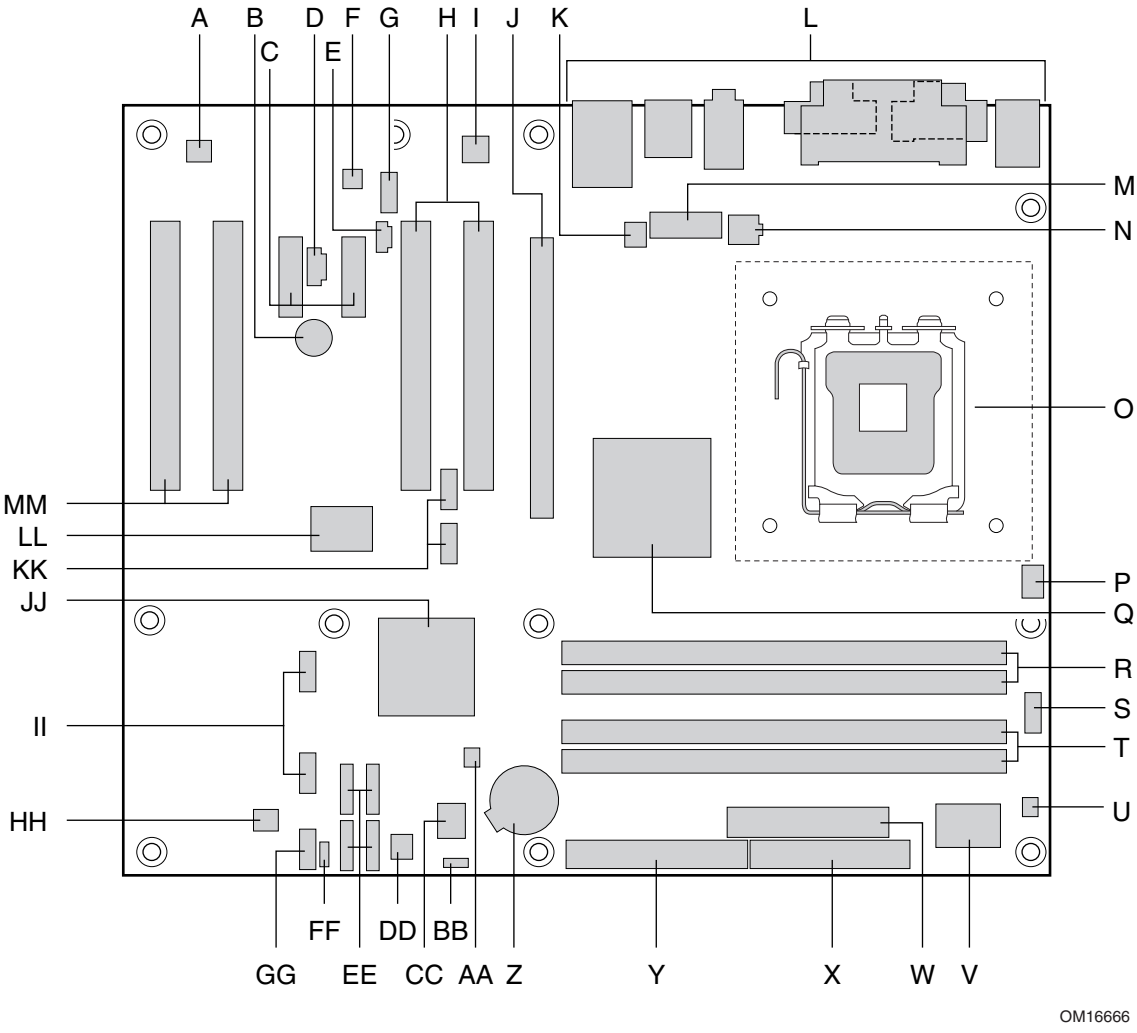


Figure 1. D915GAV Board Components

Table 4 lists the components identified in Figure 1.

Table 4. D915GAV Board Components Shown in Figure 1.

Item/callout from Figure 1	Description
A	Rear fan connector 2
B	Speaker
C	PCI Express x1 bus add-in card connectors
D	ATAPI CD-ROM connector (optional)
E	S/PDIF connector (optional)
F	Realtek ALC860 audio codec
G	Front panel audio connector
H	PCI Conventional bus add-in card connectors
I	Ethernet PLC device (optional)
J	PCI Express x16 bus add-in card connector
K	Rear chassis fan connector 1
L	Back panel connectors
M	Alternate power connector
N	+12V power connector (ATX12V)
O	LGA775 processor socket
P	Processor fan connector
Q	Intel 82915G GMCH
R	DIMM Channel A sockets
S	Serial port B connector (optional)
T	DIMM Channel B sockets
U	SCSI LED (optional)
V	I/O controller
W	Power connector
X	Diskette drive connector
Y	Parallel ATE IDE connector
Z	Battery
AA	Chassis intrusion connector
BB	BIOS Setup configuration jumper block
CC	4 Mbit Firmware Hub (FWH)
DD	Front chassis fan connector
EE	Serial ATA connectors
FF	Auxiliary front panel power LED connector
GG	Front panel connector
HH	ATX fan connector (optional)
II	Front panel USB connector
JJ	Intel 82801FB I/O Controller Hub (ICH6)
KK	Front panel IEEE-1394a connectors (optional)
LL	IEEE-1394a controller (optional)
MM	PCI Conventional bus add-in card connectors

Figure 2 shows the location of the major components on the Desktop Board D915GAG.

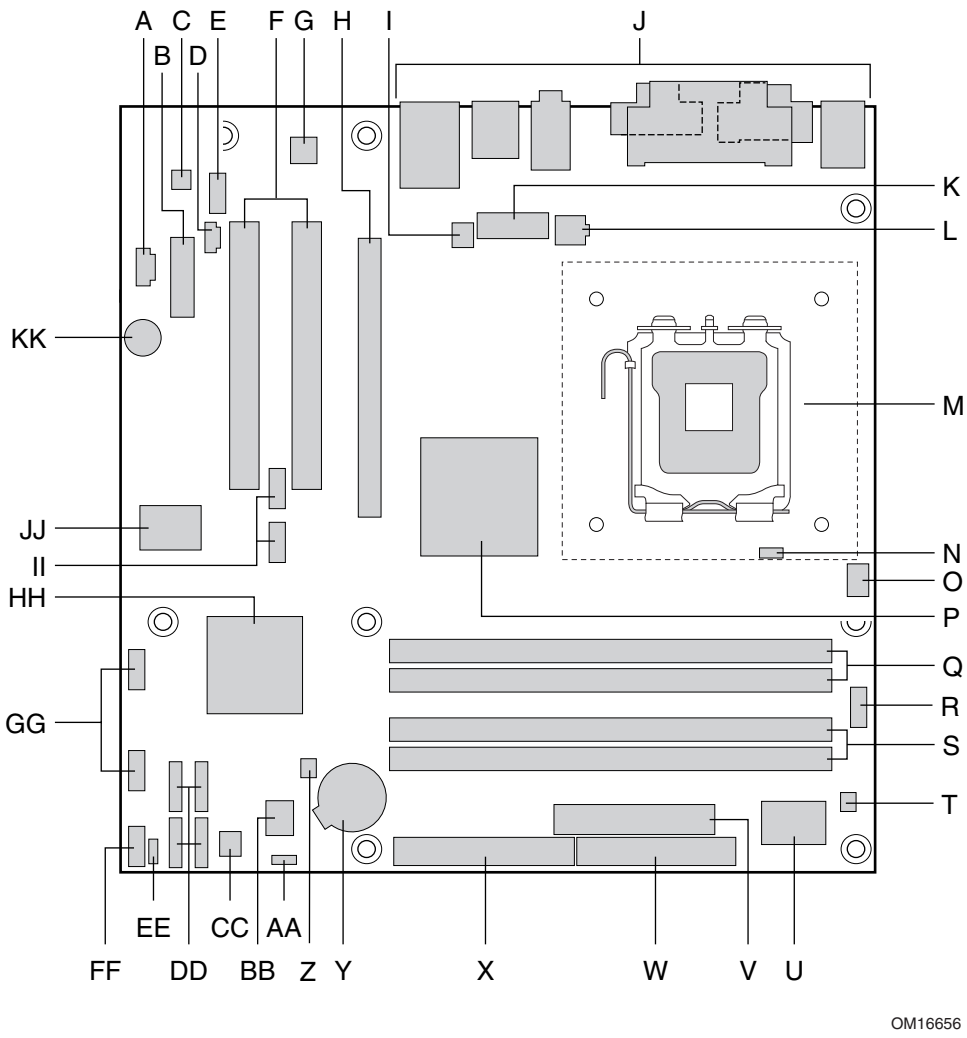


Figure 2. D915GAG Board Components

Table 5 lists the components identified in Figure 2.

Table 5. D915GAG Board Components Shown in Figure 2.

Item/callout from Figure 2	Description
A	ATAPI CD-ROM connector (optional)
B	PCI Express x1 bus add-in card connectors
C	Realtek ALC860 audio codec
D	S/PDIF connector (optional)
E	Front panel audio connector
F	PCI Conventional bus add-in card connectors
G	Ethernet PLC device (optional)
H	PCI Express x16 bus add-in card connector
I	Rear chassis fan connector
J	Back panel connectors
K	Alternate power connector
L	+12V power connector (ATX12V)
M	LGA775 processor socket
N	Hardware monitoring and fan control ASIC
O	Processor fan connector
P	Intel 82915G GMCH
Q	DIMM Channel A sockets
R	Serial port B connector (optional)
S	DIMM Channel B sockets
T	SCSI LED connector (optional)
U	I/O controller
V	Power connector
W	Diskette drive connector
X	Parallel ATE IDE connector
Y	Battery
Z	Chassis intrusion connector
AA	BIOS Setup configuration jumper block
BB	4 Mbit Firmware Hub (FWH)
CC	Front chassis fan connector
DD	Serial ATA connectors
EE	Auxiliary front panel power LED connector
FF	Front panel connector
GG	Front panel USB connector
HH	Intel 82801FB I/O Controller Hub (ICH6)
II	Front panel IEEE-1394a connectors (optional)
JJ	IEEE-1394a controller (optional)
KK	Speaker

1.3.4 Block Diagram

Figure 3 is a block diagram of the major functional areas of the boards.

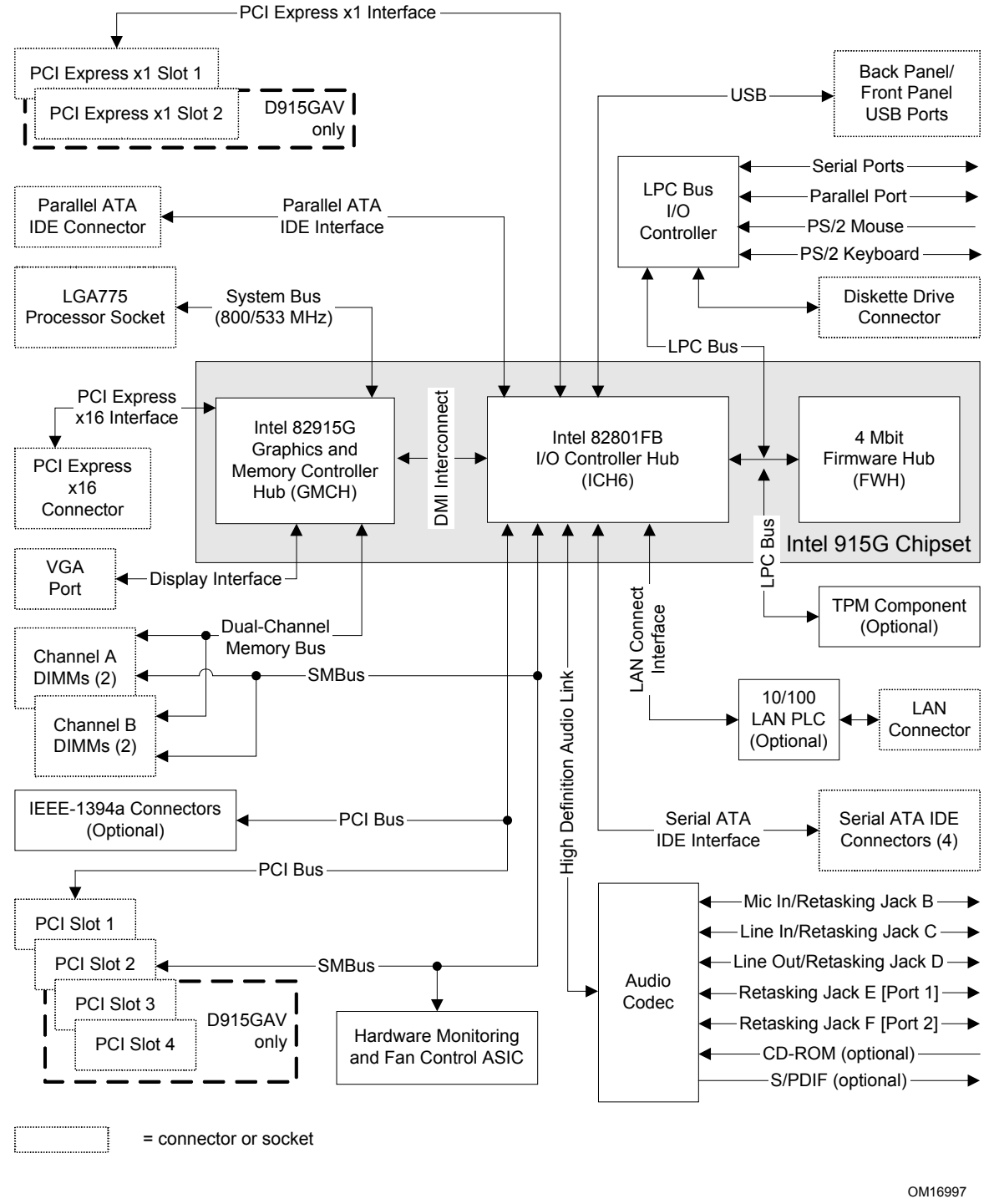


Figure 3. Block Diagram

1.4 Online Support

To find information about…	Visit this World Wide Web site:
Intel Desktop Boards D915GAV and D915GAG under "Desktop Board Products" or "Desktop Board Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the Desktop Board D915GAV	http://developer.intel.com/design/motherbd/av/av_available.htm
Available configurations for the Desktop Board D915GAG	http://developer.intel.com/design/motherbd/ag/ag_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
ICH6 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.5 Processor

The boards are designed to support Intel Pentium 4 processors in an LGA775 processor socket with an 800 or 533 MHz system bus. See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors for the D915GAV board	http://www.intel.com/design/motherbd/av/av_proc.htm
Supported processors for the D915GAG board	http://www.intel.com/design/motherbd/ag/ag_proc.htm

CAUTION

Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTE

- *Use only ATX12V-compliant power supplies.*
- *Refer to Table 6 on page 20 for a list of supported system bus frequency and memory speed combinations.*

For information about	Refer to
Power supply connectors	Section 2.8.2.2, page 70

1.6 System Memory

The boards have four DIMM sockets and support the following memory features:

- 2.5 V (only) DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:

  Double-sided DIMMS with x16 organization are not supported.
- 4 GB maximum total system memory. Refer to Section 2.2.1 on page 53 for information on the total amount of addressable memory.
- Minimum total system memory: 128 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR 400 MHz and DDR 333 MHz SDRAM DIMMs

Table 6 lists the supported system bus frequency and memory speed combinations.

Table 6. Supported System Bus Frequency and Memory Speed Combinations

To use this type of DIMM…	The processor's system bus frequency must be…
DDR 400	800 MHz
DDR 333 (Note)	800 or 533 MHz

Note: When using an 800 MHz system bus frequency processor, DDR 333 memory is clocked at 320 MHz. This minimizes system latencies to optimize system throughput.

NOTES

- *Remove the PCI Express x16 video card before installing or upgrading memory to avoid interference with the memory retention mechanism.*
- *To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

Table 7 lists the supported DIMM configurations.

Table 7. Supported Memory Configurations

DIMM Capacity	Configuration	SDRAM Density	SDRAM Organization Front-side/Back-side	Number of SDRAM Devices
128 MB	SS	256 Mbit	16 M x 16/empty	4
256 MB	SS	256 Mbit	32 M x 8/empty	8
256 MB	SS	512 Mbit	32 M x 16/empty	4
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16
512 MB	SS	512 Mbit	64 M x 8/empty	8
512 MB	SS	1 Gbit	64 M x 16/empty	4
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16
1024 MB	SS	1 Gbit	128 M x 8/empty	8
2048 MB	DS	1 Gbit	128 M x 8/128 M x 8	16

Note: In the second column, “DS” refers to double-sided memory modules (containing two rows of SDRAM) and “SS” refers to single-sided memory modules (containing one row of SDRAM).

INTEGRATOR’S NOTE

It is possible to install four 2048 MB (2 GB) modules for a total of 8 GB of system memory, however, only 4 GB of address space is available. Refer to Section 2.2.1, on page 53 for additional information on available memory.

1.6.1 Memory Configurations

The Intel 82915G GMCH supports two types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

Figure 4 illustrates the memory channel and DIMM configuration.

NOTE

The DIMM0 sockets of both channels are blue. The DIMM1 sockets of both channels are black.

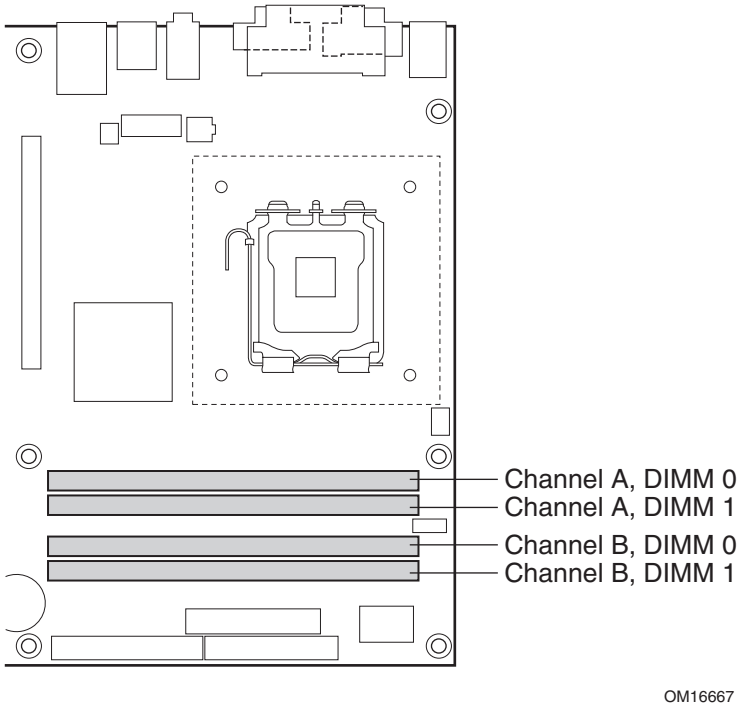


Figure 4. Memory Channel and DIMM Configuration

1.6.1.1 Dual Channel (Interleaved) Mode Configurations

Figure 5 shows a dual channel configuration using two DIMMs. In this example, the DIMM0 (blue) sockets of both channels are populated with identical DIMMs.

Figure 5. Dual Channel (Interleaved) Mode Configuration with Two DIMMs

Figure 6 shows a dual channel configuration using three DIMMs. In this example, the combined capacity of the two DIMMs in Channel A equal the capacity of the single DIMM in the DIMM0 (blue) socket of Channel B.

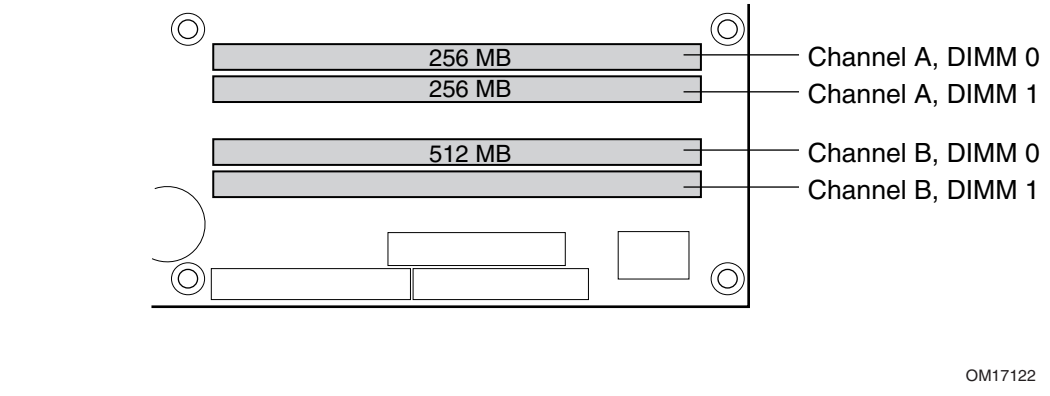


Figure 6. Dual Channel (Interleaved) Mode Configuration with Three DIMMs

Figure 7 shows a dual channel configuration using four DIMMs. In this example, the combined capacity of the two DIMMs in Channel A equal the combined capacity of the two DIMMs in Channel B. Also, the DIMMs are matched between DIMM0 and DIMM1 of both channels.

Figure 7. Dual Channel (Interleaved) Mode Configuration with Four DIMMs

1.6.1.2 Single Channel (Asymmetric) Mode Configurations

NOTE

Dual channel (Interleaved) mode configurations provide the highest memory throughput.

Figure 8 shows a single channel configuration using one DIMM. In this example, only the DIMM0 (blue) socket of Channel A is populated. Channel B is not populated.

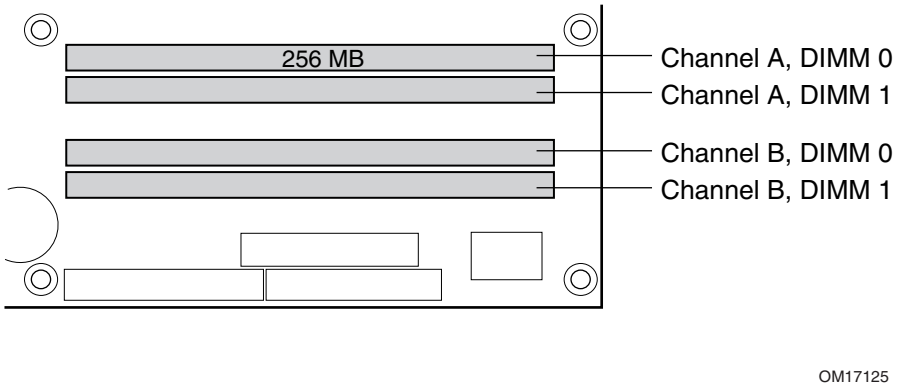


Figure 8. Single Channel (Asymmetric) Mode Configuration with One DIMM

Figure 9 shows a single channel configuration using three DIMMs. In this example, the combined capacity of the two DIMMs in Channel A does not equal the capacity of the single DIMM in the DIMM0 (blue) socket of Channel B.

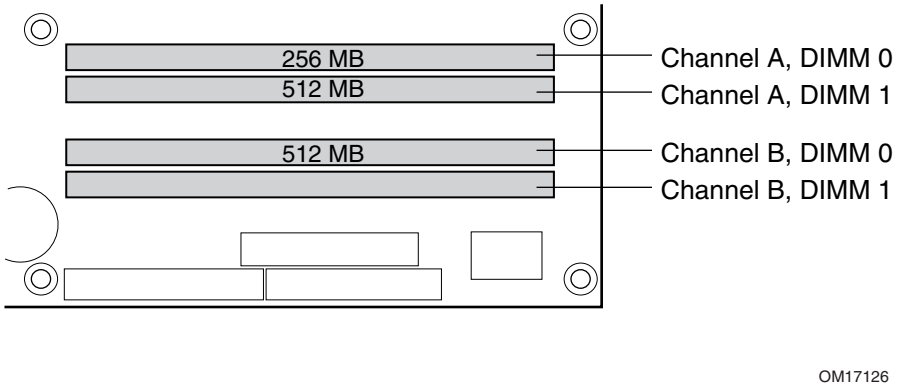


Figure 9. Single Channel (Asymmetric) Mode Configuration with Three DIMMs

1.7 Intel® 915G Chipset

The Intel 915G chipset consists of the following devices:

- Intel 82915G Graphics Memory Controller Hub (GMCH) with Direct Media Interface (DMI) interconnect
- Intel 82801FB I/O Controller Hub (ICH6) with DMI interconnect
- Firmware Hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the PCI Express bus, and the DMI interconnect. The ICH6 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS.

For information about	Refer to
The Intel 915G chipset	http://developer.intel.com/
Resources used by the chipset	Chapter 2

1.7.1 Intel 915G Graphics Subsystem

The Intel 915G chipset contains two separate, mutually exclusive graphics options. Either the GMA900 graphics controller (contained within the 82915G GMCH) is used, or a PCI Express x16 add-in card can be used. When a PCI Express x16 add-in card is installed, the GMA900 graphics controller is disabled.

1.7.1.1 Intel® GMA900 Graphics Controller

The Intel GMA900 graphics controller features the following:

- Integrated graphics controller
  - 32 bpp (Bits Per Pixel) graphics engine
  - 333 MHz core frequency
  - 256-bit 2-D engine
  - 32-bit 3-D engine
  - Motion video acceleration
  - Pixel Shader 2.0
  - 4-pixel pipes
  - DirectX* 9.0 Hardware Acceleration
  - Software Vertex Shader
- Up to 2048 x 1536 at 75 Hz refresh
- With Advanced Digital Display 2 (ADD2) card support flat panel displays up to 2048 x 1536 at 75 Hz or digital CRTs/HDTV displays at 1920 x 1080 at 85 Hz
- High performance 3-D setup and render engine
- High quality/performance texture engine
- Display
  - Integrated 24-bit 400 MHz RAMDAC
  - DDC2B compliant interface

- Video
  - — Asynchronous dual monitor display with ADD2 card
  - — Hardware motion compensation for software MPEG2 decode
  - — Two multiplexed DVO port interfaces with 200 MHz pixel clocks using an ADD2 card
- Dynamic Video Memory Technology (DVMT) support up to 224 MB
- Intel® Zoom Utility

For information about	Refer to
DVMT	Section 1.7.1.2, page 27
Obtaining graphics software and utilities	Section 1.4, page 19

1.7.1.2 Dynamic Video Memory Technology (DVMT)

DVMT enables enhanced graphics and memory performance through Direct AGP, and highly efficient memory utilization. DVMT ensures the most efficient use of available system memory for maximum 2-D/3-D graphics performance. Up to 224 MB of system memory can be allocated to DVMT on systems that have 512 MB or more of total system memory installed. Up to 128 MB can be allocated to DVMT on systems that have 256 MB but less than 512 MB of total installed system memory. Up to 64 MB can be allocated to DVMT when less than 256 MB of system memory is installed. DVMT returns system memory back to the operating system when the additional system memory is no longer required by the graphics subsystem.

DVMT will always use a minimal fixed portion of system physical memory (as set in the BIOS Setup program) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate additional system memory to the graphics buffer as needed for performing graphics functions.

NOTE

The use of DVMT requires operating system driver support.

1.7.1.3 Advanced Digital Display 2 (ADD2) Card Support

The GMCH routes two multiplexed DVO ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. The DVO ports can be paired for a dual channel configuration to support up to a 400 MHz pixel clock. When an ADD2 card is detected, the Intel GMA900 graphics controller is enabled and the PCI Express x16 connector is configured for DVO mode. DVO mode enables the DVO ports to be accessed by the ADD2 card. An ADD2 card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different color depths and resolutions. ADD2 cards can be designed to support the following configurations:

- TV-Out (composite video)
- Transition Minimized Differential Signaling (TMDS) for DVI 1.0
- Low Voltage Differential Signaling (LVDS)
- Single device operating in dual channel mode
- VGA output
- HDTV output

1.7.1.4 Configuration Modes

A list of supported modes for the Intel GMA900 graphics controller is available as a downloadable document.

For information about	Refer to
Supported modes for the D915GAV board	http://www.intel.com/design/motherbd/av/av_prdoc.htm
Supported modes for the D915GAG board	http://www.intel.com/design/motherbd/ag/ag_prdoc.htm

1.7.2 USB

The boards support up to eight USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH6 provides the USB controller for all ports. The port arrangement is as follows:

- Four ports are implemented with dual stacked back panel connectors adjacent to the audio connectors
- Four ports are routed to two separate front panel USB connectors

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 17, page 62
The location of the front panel USB connectors on the D915GAV board	Figure 18, page 64
The location of the front panel USB connectors on the D915GAG board	Figure 19, page 66

1.7.3 IDE Support

The boards provides five IDE interface connectors:

- One parallel ATA IDE connector that supports two devices
- Four serial ATA IDE connectors that support one device per connector

1.7.3.1 Parallel ATE IDE Interface

The ICH6's Parallel ATA IDE controller has one bus-mastering Parallel ATA IDE interface. The Parallel ATA IDE interface supports the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH6's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interface also supports ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The boards support Laser Servo (LS-120) diskette technology through the Parallel ATA IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the Parallel ATA IDE connector on the D915GAV board	Figure 18, page 64
The location of the Parallel ATA IDE connector on the D915GAG board	Figure 19, page 66

1.7.3.2 Serial ATA Interfaces

The ICH6's Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 150 MB/s per port. One device can be installed on each port for a maximum of four Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows* XP and Windows 2000 operating systems.

NOTE

Many Serial ATA drives use new low-voltage power connectors and require adaptors or power supplies equipped with low-voltage power connectors.

For more information, see: http://www.serialata.org/

For information about	Refer to
The location of the Serial ATA IDE connectors on the D915GAV board	Figure 18, page 64
The location of the Serial ATA IDE connectors on the D915GAG board	Figure 19, page 66

1.7.3.3 SCSI Hard Drive Activity LED Connector (Optional)

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows an add-in hard drive controller to use the same LED as the onboard IDE controller. For proper operation, this connector should be wired to the LED output of the add-in hard drive controller. The LED

indicates when data is being read from, or written to, either the add-in hard drive controller or the onboard IDE controller (Parallel ATA or Serial ATA).

For information about	Refer to
The location of the SCSI hard drive activity LED connector on the D915GAV board	Figure 18, page 64
The location of the SCSI hard drive activity LED connector on the D915GAG board	Figure 19, page 66
The signal names of the SCSI hard drive activity LED connector	Table 26, page 69

1.7.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

1.8 PCI Express Connectors

The boards provide the following PCI Express connectors:

- One PCI Express x16 connector supporting simultaneous transfer speeds up to 8 GBytes/sec
- Two PCI Express x1 connectors. The x1 interfaces support simultaneous transfer speeds up to 500 MBytes/sec

The PCI Express interface supports the PCI Conventional bus configuration mechanism so that the underlying PCI Express architecture is compatible with PCI Conventional compliant operating systems. Additional features of the PCI Express interface includes the following:

- Support for the PCI Express enhanced configuration mechanism
- Automatic discovery, link training, and initialization
- Support for Active State Power Management (ASPM)
- SMBus 2.0 support
- Wake# signal supporting wake events from ACPI S1, S3, S4, or S5
- Software compatible with the PCI Power Management Event (PME) mechanism defined in the PCI Power Management Specification Rev. 1.1

1.9 I/O Controller

The I/O controller provides the following features:

- Two serial ports (Serial Port B is optional)
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI Conventional bus systems

- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI Conventional bus power management support

The BIOS Setup program provides configuration options for the I/O controller.

1.9.1 Serial Ports

The Desktop Board can support up to two serial port connectors. Serial port A is located on the back panel. Serial port B (optional) is accessible using a connector on the component side of board. The serial ports support data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port A connector	Figure 17, page 62
The location of the serial port B connector on the D915GAV board	Figure 18, page 64
The location of the serial port B connector on the D915GAG board	Figure 19, page 66
The signal names of the serial port B connector	Table 24, page 68

1.9.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 17, page 62

1.9.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector on the D915GAV board	Figure 18, page 64
The location of the diskette drive connector on the D915GAG board	Figure 19, page 66

1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 17, page 62

1.10 Audio Subsystem

The boards support the Intel High Definition audio subsystem based on the Realtek ALC860 codec. The audio subsystem supports the following features:

- Advanced jack sense (front and rear panel) that enables the audio codec to recognize the device that is connected to an audio port. All jacks are capable of retasking according to user's definition, or can be automatically switched depending on the recognized device type.
- Stereo input and output for all jacks
- A signal-to-noise (S/N) ratio of 90 dB

INTEGRATOR'S NOTE

For the front panel jack sensing and automatic retasking feature to function, a front panel daughter card that is designed for Intel High Definition Audio must be used. Otherwise, an AC '97 style audio front panel connector will be assumed and the Line Out and Mic In functions will be permanent.

1.10.1 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.4, page 19

1.10.2 Audio Connectors

The boards contain audio connector on both the back panel and the component side of the board. The component-side audio connectors include the following:

- Front panel audio (a 2 x 5-pin connector that provides mic in and line out signals for front panel audio connectors)
- ATAPI CD-ROM (an optional 1 x 4-pin ATAPI-style connector for connecting an internal ATAPI CD-ROM drive to the audio mixer)
- S/PDIF (an optional 1 x 3 connector that provides S/PDIF output signals)

The functions of the back panel audio connectors are dependent on which subsystem is present.

For information about	Refer to
The location of the front panel audio connector, the optional ATAPI CD-ROM connector, and the optional S/PDIF connector on the D915GAV board	Figure 18, page 64
The location of the front panel audio connector, the optional ATAPI CD-ROM connector, and the optional S/PDIF connector on the D915GAG board	Figure 19, page 66
The signal names of the front panel audio connector	Table 23, page 68
The signal names of the optional ATAPI CD-ROM connector	Table 22, page 68
The signal names of the optional S/PDIF connector	Table 21, page 68

1.10.3 Intel® High Definition Audio Subsystem

The Intel High Definition Audio subsystem includes the following:

- Intel 82801FB I/O Controller Hub (ICH6)
- Realtek ALC860 audio codec
- Microphone input that supports a single dynamic, condenser, or electret microphone

The front and back audio connectors are configurable through the audio device drivers. The available configurable audio ports are shown in Figure 10.

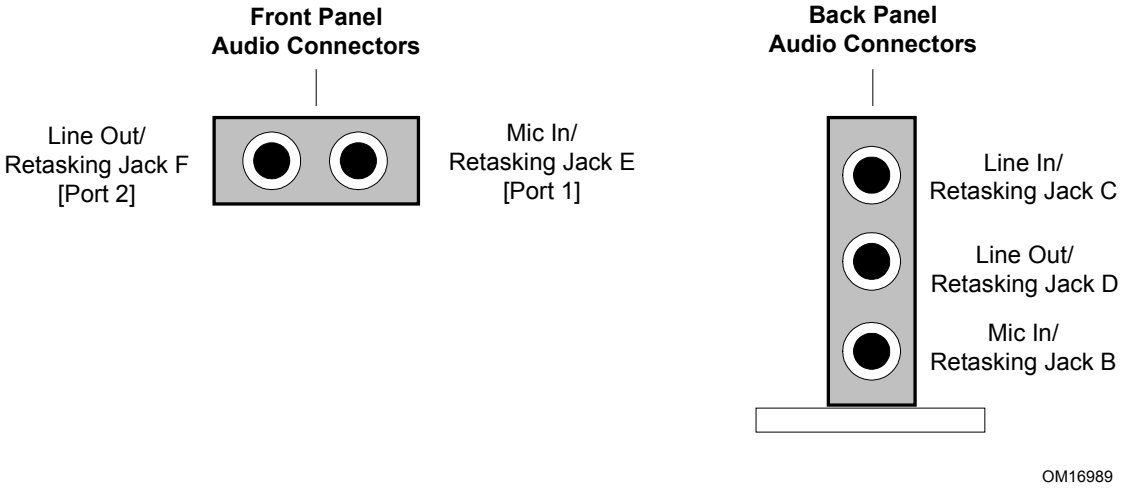


Figure 10. Front/Back Panel Audio Connector Options for High Definition Audio Subsystem

Figure 11 is a block diagram of the High Definition audio subsystem.

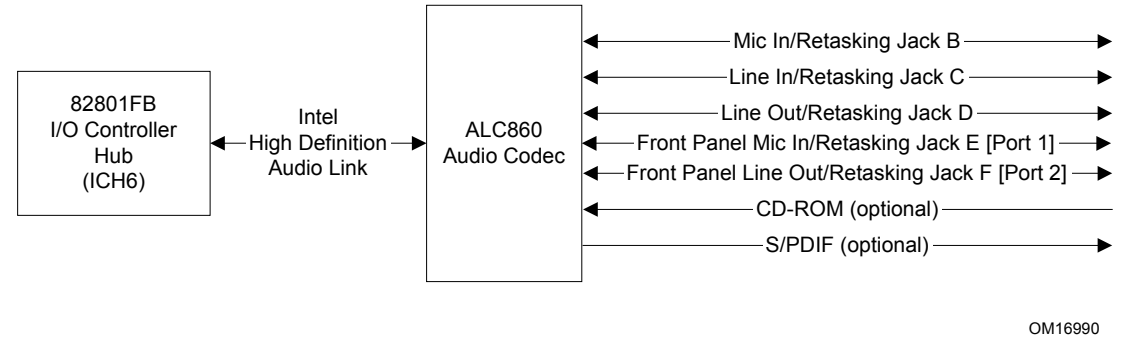


Figure 11. High Definition Audio Subsystem Block Diagram

For information about	Refer to
The back panel audio connectors	Figure 17, page 62

1.11 LAN Subsystem

The 10/100 Mbits/sec LAN subsystem consists of the following:

- The Intel 82801FB ICH6
- An Intel 82562EZ Platform LAN Connect (PLC) device for 10/100 Mbits/sec Ethernet LAN connectivity
- An RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN Connect Interface (LCI) between the 82562EZ and the ICH6
- PCI Conventional bus power management
  - — Supports ACPI technology
  - — Supports LAN wake capabilities

1.11.1 Intel® 82562EZ Physical Layer Interface Device

The Intel 82562EZ provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 12 below).

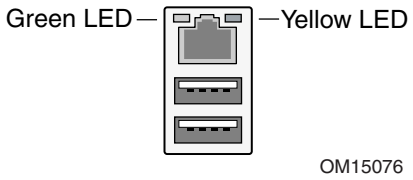


Figure 12. LAN Connector LED Locations

Table 8 describes the LED states when the board is powered up and the 10/100 Mbits/sec LAN subsystem is operating.

Table 8. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	LAN link is not established.
	On	LAN link is established.
	Blinking	LAN activity is occurring.
Yellow	Off	10 Mbits/sec data rate is selected.
	On	100 Mbits/sec data rate is selected.

1.11.3 Alert Standard Format (ASF) Support

The boards provide the following ASF support for PCI Express x1 bus add-in LAN cards and PCI Conventional bus add-in LAN cards installed in PCI Conventional bus slot 2:

- Monitoring of system firmware progress events, including:
  - BIOS present
  - Primary processor initialization
  - Memory initialization
  - Video initialization
  - PCI resource configuration
  - Hard-disk initialization
  - User authentication
  - Starting operating system boot process
- Monitoring of system firmware error events, including:
  - Memory missing
  - Memory failure
  - No video device
  - Keyboard failure
  - Hard-disk failure
  - No boot media
- Boot options to boot from different types of boot devices
- Reset, shutdown, power cycle, and power up options

1.11.4 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.4, page 19

1.11.5 Intel® Wireless Connect Technology (Optional)

Intel Wireless Connect Technology is available for Intel 82801FBW (ICH6W) based SKUs that use an Intel® PRO/Wireless 2225BG add-in card. Intel Wireless Connect Technology enables any desktop PC to join a wireless network or provide wireless Access Point services to a home or small office network through a wireless configuration wizard. Intel Wireless Connect Technology features the following:

- Wireless LAN protocols 802.11 b, g
- 11 Mbps performance with 802.11b
- 54 Mbps performance with 802.11g
- WEP, WPA (TKIP/802.1x), and MAC Address filtering for security
- Wi-Fi and WHQL certified
- Integrated Access Point that can support up to 16 clients

1.12 Hardware Management Subsystem

The hardware management features enable the Desktop Boards to be compatible with the Wired for Management (WfM) specification. The Desktop Board has several hardware management features, including the following:

- Fan monitoring and control (through the hardware monitoring and fan control ASIC)
- Thermal and voltage monitoring
- Chassis intrusion detection

1.12.1 Hardware Monitoring and Fan Control ASIC

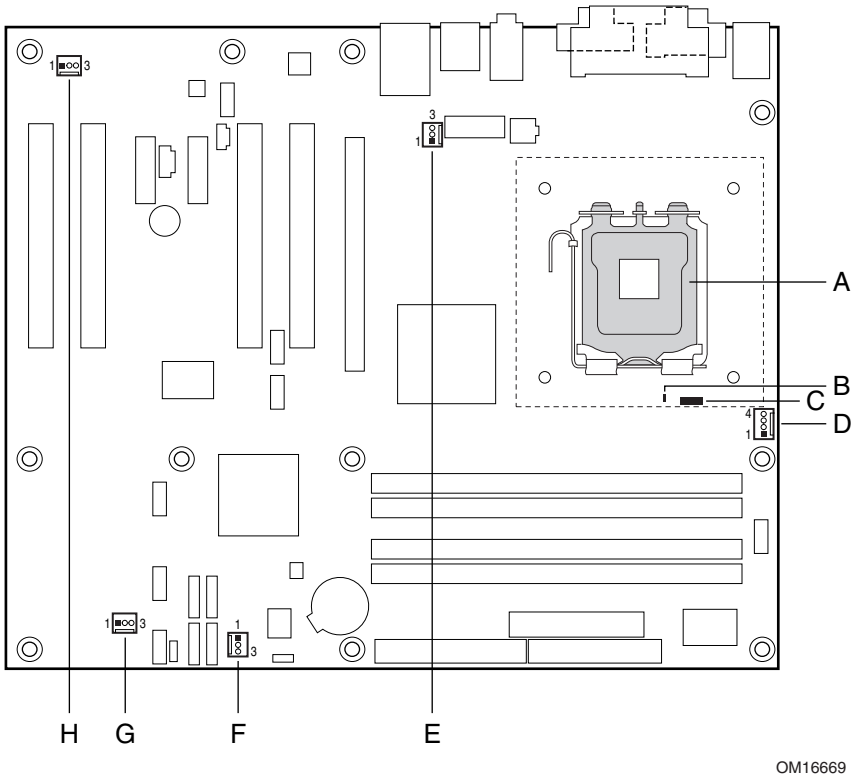
The features of the hardware monitoring and fan control ASIC include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 VSB, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface

For information about	Refer to
The location of the fan connectors and sensors for thermal monitoring on the D915GAV board	Figure 13, page 37
The location of the fan connectors and sensors for thermal monitoring on the D915GAG board	Figure 14, page 38

1.12.2 Thermal Monitoring

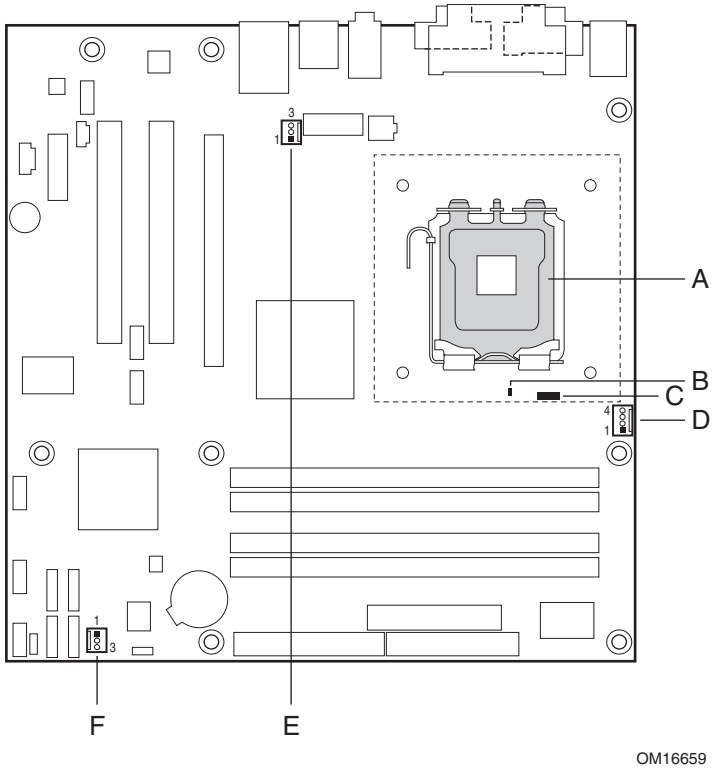
Figure 13 shows the location of the sensors and fan connectors for the D915GAV board.



Item	Description
A	Thermal diode, located on processor die
B	Remote ambient temperature sensor
C	Ambient temperature sensor, internal to hardware monitoring and fan control ASIC
D	Processor fan
E	Rear chassis fan 1
F	Front chassis fan
G	ATX fan (optional)
H	Rear chassis fan 2

Figure 13. Thermal Monitoring for D915GAV Board

Figure 14 shows the location of the sensors and fan connectors for the D915GAG board.



Item	Description
A	Thermal diode, located on processor die
B	Remote ambient temperature sensor
C	Ambient temperature sensor, internal to hardware monitoring and fan control ASIC
D	Processor fan
E	Rear chassis fan
F	Front chassis fan

Figure 14. Thermal Monitoring for D915GAG Board

1.12.3 Fan Monitoring

Fan monitoring can be implemented using Intel® Desktop Utilities, LANDesk* software, or third-party software. The level of monitoring and control is dependent on the hardware monitoring ASIC used with the Desktop Board.

For information about	Refer to
The functions of the fan connectors	Section 1.13.2.2, page 43

1.12.4 Chassis Intrusion and Detection

The boards support a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with these boards requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 11 on page 42)
- Support for a front panel power and sleep mode switch

Table 9 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 9. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 10 lists the power states supported by the boards along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 10. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 11 lists the devices or specific events that can wake the computer from specific states.

Table 11. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note)
Modem (back panel Serial Port A)	S1, S3
PME# signal	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
USB	S1, S3
WAKE# signal	S1, S3, S4, S5

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The boards provide several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support
- WAKE# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the main power connector on the D915GAV board	Figure 18, page 64
The location of the main power connector on the D915GAG board	Figure 19, page 66
The signal names of the main power connector	Table 30, page 70

1.13.2.2 Fan Connectors

The function/operation of the fan connectors is as follows:

- The fans are on when the board is in the S0 or S1 state.
- The fans are off when the board is off or in the S3, S4, or S5 state.
- Each fan connector is wired to a fan tachometer input of the hardware monitoring and fan control ASIC.
- All fan connectors support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed.
- All fan connectors have a +12 V DC connection.

For information about	Refer to
The location of the fan connectors on the D915GAV board	Figure 18, page 64
The location of the fan connectors on the D915GAG board	Figure 19, page 66
The location of the fan connectors and sensors for thermal monitoring on the D915GAV board	Figure 13, page 37
The location of the fan connectors and sensors for thermal monitoring on the D915GAG board	Figure 14, page 38
The signal names of the processor fan connector	Table 28, page 69
The signal names of the chassis fan connectors	Table 29, page 69

1.13.2.3 LAN Wake Capabilities

⚠ CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the boards support LAN wake capabilities with ACPI in the following ways:

- The PCI Express WAKE# signal
- The PCI Conventional bus PME# signal for PCI 2.2 compliant LAN designs
- The onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

⚠ CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the boards to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 11 on page 42 lists the devices and events that can wake the computer from the S3 state.

The boards support the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards, PCI Express add-in cards, and drivers.

1.13.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.13.2.6 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

✎ NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.7 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.13.2.8 PME# Signal Wake-up Support

When the PME# signal on the PCI Conventional bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

1.13.2.9 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state.

1.13.2.10 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 15 shows the location of the standby power indicator LED in the D915GAV board. The LED is in the same location on the D915GAG board.

⚠ CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

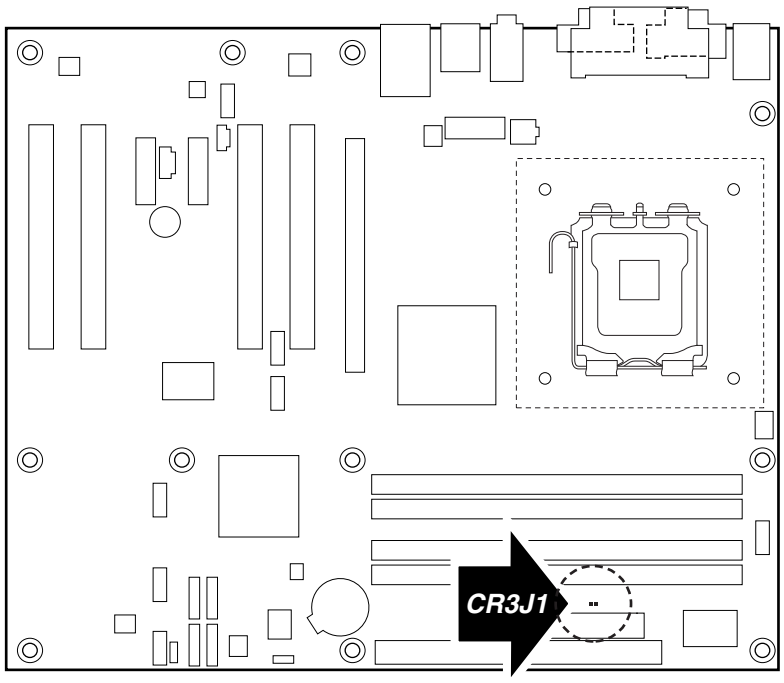


Figure 15. Location of the Standby Power Indicator LED

1.14 Trusted Platform Module (Optional)

The optional Trusted Platform Module (TPM) is a component on the desktop board that is specifically designed to enhance platform security above-and-beyond the capabilities of today's software by providing a protected space for key operations and other security critical tasks. Using both hardware and software, the TPM protects encryption and signature keys at their most vulnerable stages—operations when the keys are being used unencrypted in plain-text form. The TPM is specifically designed to shield unencrypted keys and platform authentication information from software-based attacks.

1.14.1 System Requirements

- Intel Desktop Board D915GAV or D915GAG
- Microsoft Windows 2000 Professional (SP4) or Microsoft Windows XP Professional (SP1)
- NTFS file system required
- Microsoft Internet Explorer* 5.5 or later
- Adobe* Acrobat* 5.0 or later

1.14.2 Warning of Potential Data Loss

⚠ CAUTION

Failure to follow the instructions below may cause you to lose data. Read and follow these instructions prior to Trusted Platform Module initialization.

System integrators, owners, and end users must take precautions to mitigate the chance of data loss. Data encrypted by any program utilizing the Trusted Platform Module (TPM) may become inaccessible or unrecoverable if any of the following occurs:

- Lost Password: Loss of any of the passwords associated with the TPM will render encrypted data inaccessible. No password recovery is available. **Read the Security Precautions for Password Procedures**.
- Hard Drive Failure: In the event of a failure of a hard disk (or other storage media) that contains encrypted data, an image of the hard disk (or other storage media) must be restored from backup before access to encrypted data may become available. The owner/user should backup the system hard disk on a regular basis. **Read the Security Precautions below for Hard Drive Backup Procedures**.
- Platform Failure: In the event of a platform failure and/or replacement of the motherboard, recovery procedures may allow migratable keys to be recovered and may restore access to encrypted data. All non-migratable keys and their associated data will be lost. Both the Infineon* Security Platform software and Wave Systems* EMBASSY* Trust Suite utilize migratable keys. Please check any other software that accesses the TPM for migratability. **Read the Security Precautions for Emergency Recovery File Back Up Procedures**.
- Loss of Trusted Platform Module Ownership: Trusted Platform Module Ownership/contents may be cleared (via a BIOS switch) to allow for the transfer of a system to a new owner. If TPM ownership is cleared, either intentionally or in error, recovery procedures may allow the migratable keys to be recovered and may restore access to encrypted data. **Read the Security Precautions for Emergency Recovery File Back Up Procedures**.

1.14.3 Security Precautions

Security, like any other aspect of computer maintenance requires planning. What is unique about security has to do with understanding who "friends" and adversaries are. The TPM provides mechanisms to enable the owner/user to protect their information from adversaries. To provide this protection the TPM effectively puts "locks" around the data. Just like physical locks, if keys or combinations are lost, the assets (i.e., data) may be inaccessible not only to adversaries, but also to asset owner/user.

The TPM provides two classes of keys: migratable and non-migratable. Migratable keys are designed to protect data that can be used (i.e., unencrypted) on more than one platform. This has the advantage of allowing the key data to be replicated (backed-up and restored) to another platform. This may be because of user convenience (someone uses more than one platform, or the data needs to be available to more than one person operating on different platforms). This type of key also has the advantage in that it can be backed-up and restored from a defective platform onto a new platform. However, migratable keys may not be the appropriate level of protection (e.g., the user wants the data restricted to a single platform) needed for the application. This requires a non-migratable key. Non-migratable keys carry with them a usage deficit in that while the key may be backed-up and restored (i.e., protected from hard disk failure) they are not protected against system or TPM failure. The very nature of a non-migratable key is that they can be used on one and only one TPM. In the event of a system or TPM failure, all non-migratable keys and the data associated with them will be inaccessible and unrecoverable.

⚠ CAUTION

The following precautions and procedures may assist in recovering from any of the previously listed situations. Failure to implement these security precautions and procedures may result in unrecoverable data loss.

1.14.3.1 Password Procedures

The Infineon Security Platform software allows users to configure passwords from 6 to 255 characters. A good password should consist of:

- At least one upper case letter (A to Z)
- At least one numerical character (0 to 9)
- At least one symbol character (!, @, &, etc.)

Example Passwords: “I wear a Brown hat 2 worK @ least once-a-month” or “uJGFak&%)adf35a9m”

✎ NOTE

Avoid using names or dates that can be easily guessed such as: birthdays, anniversaries, family member names, pet names, etc.

All passwords associated with the Infineon Security Platform software (Owner, Emergency Recovery Token, and User passwords) and the Wave Systems EMBASSY Trust Suite are NOT RECOVERABLE and cannot be reset without the original text. The system owner should document all passwords, store them in a secured location (vault, safe deposit box, off-site storage, etc.), and have them available for future use. These documents should be updated after any password changes.

1.14.3.2 Emergency Recovery File Back Up Procedures

The Emergency Recovery Token (**SPEmRecToken.xml**) must be saved or moved to a removable media (floppy, USB drive, CDR, flash media, etc). Once this is done, the removable media should be stored in a secure location. DO NOT LEAVE ANY COPIES of the Emergency Recovery Token on the hard drive or within any hard drive image backups. If a copy of the Emergency Recovery Token remains on the system, it could be used to compromise the Trusted Platform Module and platform.

After completing the Infineon Security Platform User Initialization Wizard, a copy of the Emergency Recovery Archive (**SPEmRecArchive.xml**) should be copied to a removable media and stored in a secure location. This procedure should be repeated after any password changes or the addition of a new user.

1.14.3.3 Hard Drive Image Backup Procedures

To allow for emergency recovery from a hard drive failure, frequent images of the hard drive should be created and stored in a secure location. In the event of a hard drive failure, the latest image can be restored to a new hard drive and access to the encrypted data may be re-established.

NOTE

All encrypted and unencrypted data that was added after the last image was created will be lost.

1.14.3.4 Clear Text Backup (Optional)

It is recommended that system owners follow the *Hard Drive Image Backup Procedures*. To backup select files without creating a drive image, files can be moved from secured programs or drive letters to an unencrypted directory. The unencrypted (clear text) files may then be backed up to a removable media and stored in a secure location. The advantage of the clear text backup is that no TPM key is required to restore the data. This option is not recommended because the data is exposed during backup and restore.

1.14.4 Trusted Platform Module Ownership

The Trusted Platform Module is disabled by default when shipped and the owner/end customer of the system assumes “ownership” of the TPM. This permits the owner of the system to control initialization of the TPM and create all the passwords associated with the TPM that is used to protect their keys and data.

System builders/integrators may install both the Infineon Security Platform software and the Wave System EMBASSY Trust Suite, but SHOULD NOT attempt to use or activate the TPM or either software package.

1.14.5 Enabling the Trusted Platform Module

The Trusted Platform Module is disabled by default when shipped to insure that the owner/end customer of the system initializes the TPM and configures all security passwords. The owner/end customer should use the following steps to enable the TPM.

1. While the PC is displaying the splash screen (or POST screen), press the <F2> key to enter BIOS.
2. Use the arrow keys to go to the Advanced Menu, select Peripheral Configuration, and then press the <Enter> key.
3. Select the Trusted Platform Module, press <Enter>, and select Enabled and press <Enter> again (display should show: `Trusted Platform Module [Enabled]`).
4. Press the <F10> key, select Ok and press <Enter>.
5. System should reboot and start Microsoft Windows.

1.14.6 Assuming Trusted Platform Module Ownership

Once the TPM has been enabled, ownership must be assumed by using the Infineon Security Platform Software. The owner/end user should follow the steps listed below to take ownership of the TPM:

1. Start the system.
2. Launch the Infineon Security Platform Initialization Wizard.
3. Create Owner password (before creating any password, review the Password Recommendations made earlier in this document).
4. Create a new Recovery Archive (note the file name and location).
5. Specify a Security Platform Emergency Recovery Token password and location. (this password should not match the Owner password or any other password).
6. Define where to save the Emergency Recovery Token (note the file location and name).
7. The software will then create recovery archive files and finalize ownership of the TPM.
8. After completing the Infineon Security Platform Initialization Wizard, the Emergency Recovery Token (**SPEmRecToken.xml**) must be moved to a removable media (floppy, CDR, flash media, etc) if the file was not saved to a removable media during installation. Once this is done, the removable media should be stored in a secure location. No copies of this Emergency Recovery Token file should remain on the system. If a copy remains on the system, it could be used to compromise the security of the platform.
9. Launch the Infineon Security Platform User Initialization Wizard.
10. Create a Basic User password (this password is the most frequently used and should not match any other password).
11. Select and configure Security Platform features for this user.
12. After completing the Infineon Security Platform User Initialization Wizard, a copy of the Emergency Recovery Archive (**SPEmRecArchive.xml**) should be copied to a removable media and stored in a secure location. This procedure should be repeated after any password changes or the addition of new users.
13. Restart the system.
14. To backup the keys for the EMBASSY Trust Suite, the Key Transfer Manager software must be configured. Launch the Key Transfer Manager from the program menu.
15. Follow the instructions and create and document the locations for both the archive and restoration key files. The key archive should be located on a removable media and stored in a secure location when not in use.
16. Create and document the password to protect the key archive.
17. Provide the TPM Owner password to allow the Key Transfer Manager to create the archive and restoration key files.

18. Upon completing the configuration of the Key Transfer Manager, it will place an icon in the task bar and automatically back up all new and updated keys associated with the EMBASSY Trust Suite. If the removable media that contains the archive file is not present when a new key is generated, then keys will have to be manually backed up using the Key Transfer Manager when the removable media is available.
19. All passwords associated with the Infineon Security Platform Software (Owner, Emergency Recovery Token, and User passwords) and Wave Systems EMBASSY Trust Suite and Key Transfer Manager are not recoverable and cannot be reset without the original text. These passwords should be documented and stored in a secured location (vault, safe deposit box, off-site storage, etc.) in case they are needed in the future. These documents and files should be updated after any password changes.

1.14.7 Recovery Procedures

1.14.7.1 Recovering from Hard Disk Failure

Restore the latest hard drive image from backup to the new hard drive – no TPM specific recovery is necessary.

1.14.7.2 Recovering from Desktop Board or TPM Failure

This procedure may restore the migratable keys from the Emergency Recovery Archive, and does not restore any previous keys or content to the TPM. This recovery procedure may restore access to the Infineon Security Platform software and Wave Systems EMBASSY Trust Suite that are secured with migratable keys.

Requirements:

- Emergency Recovery Archive (created with the Infineon Security Platform Initiation Wizard)
- Emergency Recovery Token (created with the Infineon Security Platform Initiation Wizard)
- Emergency Recovery Token Security Password (created with the Infineon Security Platform Initiation Wizard)
- Working original operating system (OS) installation, or a restored image of the hard drive
- Wave Systems Key Transfer Manager archive password
- TPM Ownership password

This recovery procedure only restores the migratable keys from the previously created Recovery Archives.

1. Replace the desktop board with the same model as the failed board.
2. Start the original operating system or restore the original hard drive image.
3. Start the Infineon Security Platform Initialization Wizard and check the “I want to restore the existing Security Platform” box.
4. Follow the instructions during the Security Platform Initialization, and append the Emergency Recovery Archive to the existing archive.
5. Provide all the necessary passwords, files, and file locations as requested. It may take up to 20 minutes for Security Platform Initialization Wizard to restore the security platform settings.
6. Start User Initialization Wizard. Select “Recover Your Basic User Key” when prompted. Specify the original Basic User Key password and proceed with the wizard.

7. When re-configuring the Personal Secure Drive, select “I want to change my Personal Secure Drive setting”, confirm the drive letter and name are correct, and then proceed through the rest of the wizard.
8. Restart the system when requested.
9. To restore access to the EMBASSY Trust Suite, right mouse click on the Key Transfer Manager icon located in the taskbar in the lower right corner of the screen, and select Restore TPM Keys.
10. Provide all the necessary passwords, files, and file locations as requested by the Key Transfer Manager.
11. Upon successful completion of all steps, you should be able to access previously encrypted files.

1.14.8 Clearing Trusted Platform Module Ownership

WARNING

Disconnect the desktop board's power supply from its AC power source before you connect or disconnect cables, or install or remove any board components. Failure to do this can result in personal injury or equipment damage. Some circuitry on the desktop board can continue to operate even though the front panel power switch is off.

CAUTION

DATA ENCRYPTED BY ANY PROGRAM UTILIZING THE TPM WILL BECOME INACCESSIBLE IF TPM OWNERSHIP IS CLEARED. *Recovery procedures may allow the migratable keys to be recovered and might restore access to encrypted data. (Review the Recovery Procedures for detailed instructions).*

The TPM may be cleared to transfer ownership of the platform to a new owner.

1. Observe precautions in the above WARNING then open the system case.
2. Move the configuration jumper on the board to pins 2-3.
3. Restore power to the PC and power on.
4. System should automatically enter BIOS setup.
5. Use the arrow keys to select Clear Trusted Platform Module, press <Enter>.
6. If you agree to the warning message select Ok and press <Enter>.
7. Press the <F10> key to save and exit, select Ok and press <Enter>.
8. Power off the system.
9. Review precautions in the WARNING above.
10. Restore the configuration jumper on the board to pins 1-2.

When cleared, the TPM module is disabled by default.

1.14.9 Software Support

- For assistance with the Infineon Security Platform Software, visit the web at:

  http://www.infineon.com

- For assistance with the Wave System EMBASSY Trust Suite, visit the web at:

http://www.wave.com/support/ets.html

- For additional information about TPM and enhancing PC security, visit: https://www.trustedcomputinggroup.org/home

2 Technical Reference

What This Chapter Contains

2.1 Introduction 53
2.2 Memory Resources 53
2.3 DMA Channels 55
2.4 Fixed I/O Map 56
2.5 PCI Configuration Space Map 57
2.6 Interrupts 58
2.7 PCI Conventional Interrupt Routing Map 59
2.8 Connectors 61
2.9 Jumper Block 75
2.10 Mechanical Considerations 76
2.11 Electrical Considerations 79
2.12 Thermal Considerations 81
2.13 Reliability 83
2.14 Environmental 84
2.15 Regulatory Compliance 85

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 lists the DMA channels, Table 14 shows the I/O map, Table 15 defines the PCI Conventional bus configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Resources

2.2.1 Addressable Memory

The board utilizes 4 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (firmware hub), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 4 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/firmware hub (2 MB)
- Local APIC (19 MB)
- Digital Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express configuration space (256 MB)
- MCH base address registers, internal graphics ranges, PCI Express ports (up to 512 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Conventional and PCI Express add-in cards

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. Figure 16 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

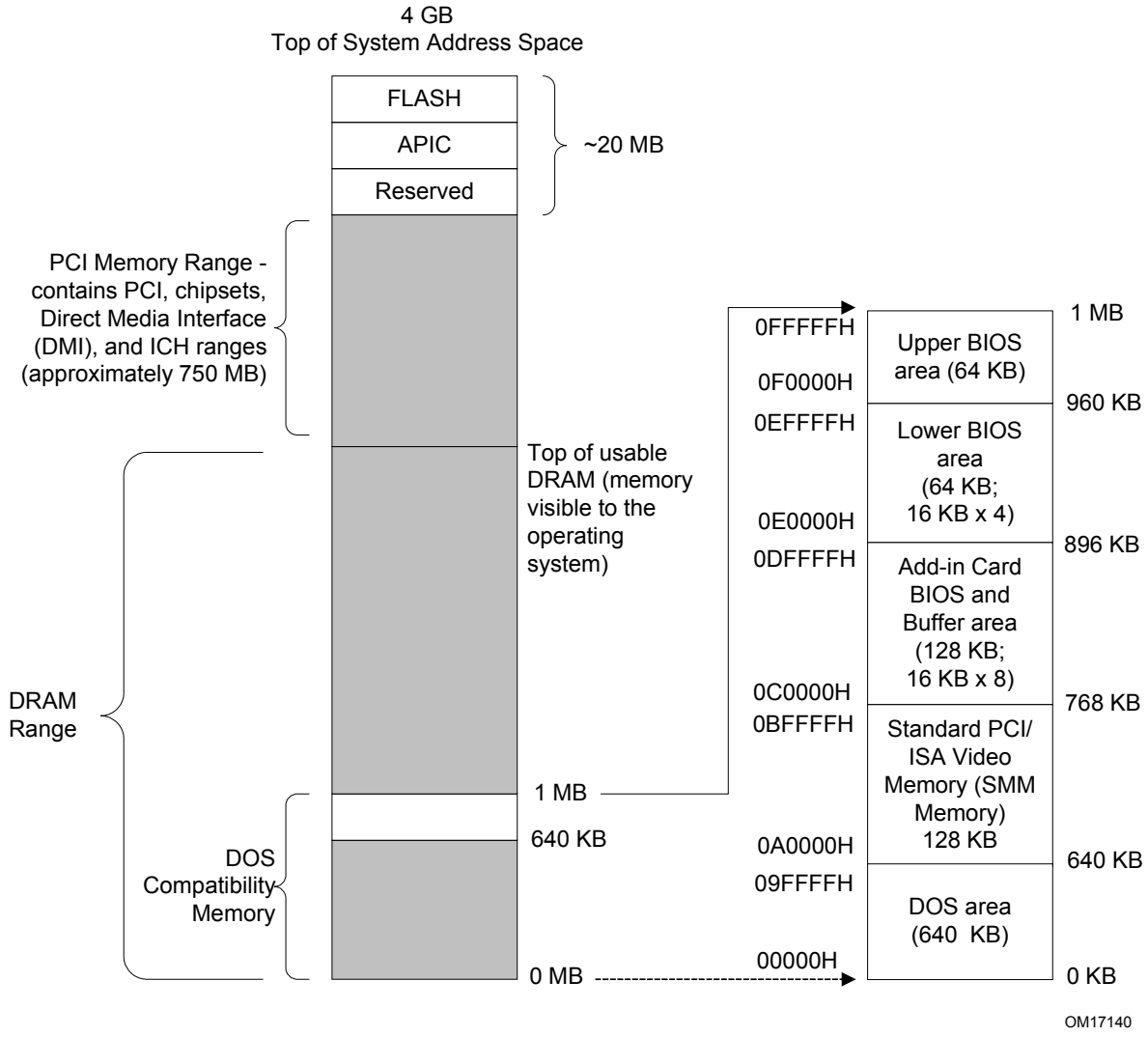


Figure 16. Detailed System Memory Address Map

2.2.2 Memory Map

Table 12 lists the system memory map.

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 4194304 K	100000 - FFFFFFFF	4095 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI Conventional bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 DMA Channels

Table 13. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.4 Fixed I/O Map

Table 14. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D915GAV/D915GAG. Refer to the ICH6 data sheet for dynamic addressing information.
0170 - 0177	8 bytes	Secondary Parallel ATA IDE channel command block
01F0 - 01F7	8 bytes	Primary Parallel ATA IDE channel command block
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0374 - 0377	4 bytes	Secondary Parallel ATA IDE channel control block
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel
03F4 – 03F7	1 byte	Primary Parallel ATA IDE channel control block
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI Conventional bus configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI Conventional bus configuration data register
FFA0 - FFA7	8 bytes	Primary Parallel ATA IDE bus master registers
FFA8 - FFAF	8 bytes	Secondary Parallel ATA IDE bus master registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH6 address aliassing. The ICH6 data sheet provides more information on address aliassing.

For information about	Refer to
Obtaining the ICH6 data sheet	Section 1.4, page 19

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82915G component
00	01	00	PCI Express x16 graphics port (Note 1)
00	02	00	Integrated graphics controller
00	02	01	Integrated graphics controller
00	1B	00	Intel High Definition Audio Controller
00	1C	00	PCI Express port 1 (PCI Express x1 bus connector 1)
00	1C	01	PCI Express port 2
00	1C	02	PCI Express port 3 (PCI Express x1 bus connector 2) (Note 2)
00	1C	03	PCI Express port 4 (not used)
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	03	USB UHCI controller 4
00	1D	07	EHCI controller
00	1E	00	PCI bridge
00	1F	00	PCI controller
00	1F	01	Parallel ATA IDE controller
00	1F	02	Serial ATA controller
00	1F	03	SMBus controller
(Note 3)	00	00	PCI Conventional bus connector 1
(Note 3)	01	00	PCI Conventional bus connector 2
(Note 3)	02	00	PCI Conventional bus connector 3 (Note 2)
(Note 3)	03	00	PCI Conventional bus connector 4 (Note 2)
(Note 3)	08	00	Intel 82562EZ 10/100 Mbits/sec LAN PLC

Notes:

1. Present only when a PCI Express x16 graphics card is installed.
2. Not present on the D915GAG board.
3. Bus number is dynamic and can change based on add-in cards used.

2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH6 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	User available
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE/Serial ATA (if present, else user available)
15	Secondary IDE/Serial ATA (if present, else user available)
16 (Note 2)	User available (through PIRQA)
17 (Note 2)	User available (through PIRQB)
18 (Note 2)	User available (through PIRQC)
19 (Note 2)	User available (through PIRQD)
20 (Note 2)	User available (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.7 PCI Conventional Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI Conventional bus connectors and onboard PCI Conventional devices. The PCI Conventional specification describes how interrupts can be shared between devices attached to the PCI Conventional bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI Conventional device should not share an interrupt with other PCI Conventional devices. Use the following information to avoid sharing an interrupt with a PCI Conventional add-in card.

PCI Conventional devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH6 has eight Programmable Interrupt Request (PIRQ) input signals. All PCI Conventional interrupt sources either onboard or from a PCI Conventional add-in card connect to one of these PIRQ signals. Some PCI Conventional interrupt sources are electrically tied together on the board and therefore share the same interrupt. Table 17 shows an example of how the PIRQ signals are routed.

For example, using Table 17 as a reference, assume an add-in card using INTA is plugged into PCI Conventional bus connector 3. In PCI bus connector 3, INTA is connected to PIRQB, which is already connected to the ICH6 audio controller. The add-in card in PCI Conventional bus connector 3 now shares an interrupt with the onboard interrupt source.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH6 PIRQ Signal Name							
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**	**PIRQE**	**PIRQF**	**PIRQG**	**PIRQH**
ICH6 LAN					INTA			
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2					INTC	INTB	INTA	INTD
PCI bus connector 3 (Note)	INTD	INTC	INTA	INTB				
PCI bus connector 4 (Note)			INTB	INTA		INTC	INTD	

Note: Not present on the D915GAG board.

NOTE

In PIC mode, the ICH6 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 16 for the allocation of PIRQ lines to IRQ signals in APIC mode.

PCI interrupt assignments to the USB ports, Serial ATA ports, and PCI Express ports are dynamic.

2.8 Connectors

CAUTION

Only the following connectors have overcurrent protection: back panel USB, front panel USB, and PS/2.

The other internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into these groups:

- Back panel I/O connectors (see page 62)
- Component-side I/O connectors (see page 64)

2.8.1 Back Panel Connectors

Figure 17 shows the location of the back panel connectors. The back panel connectors are color-coded. The figure legend (Table 18) lists the colors used (when applicable).

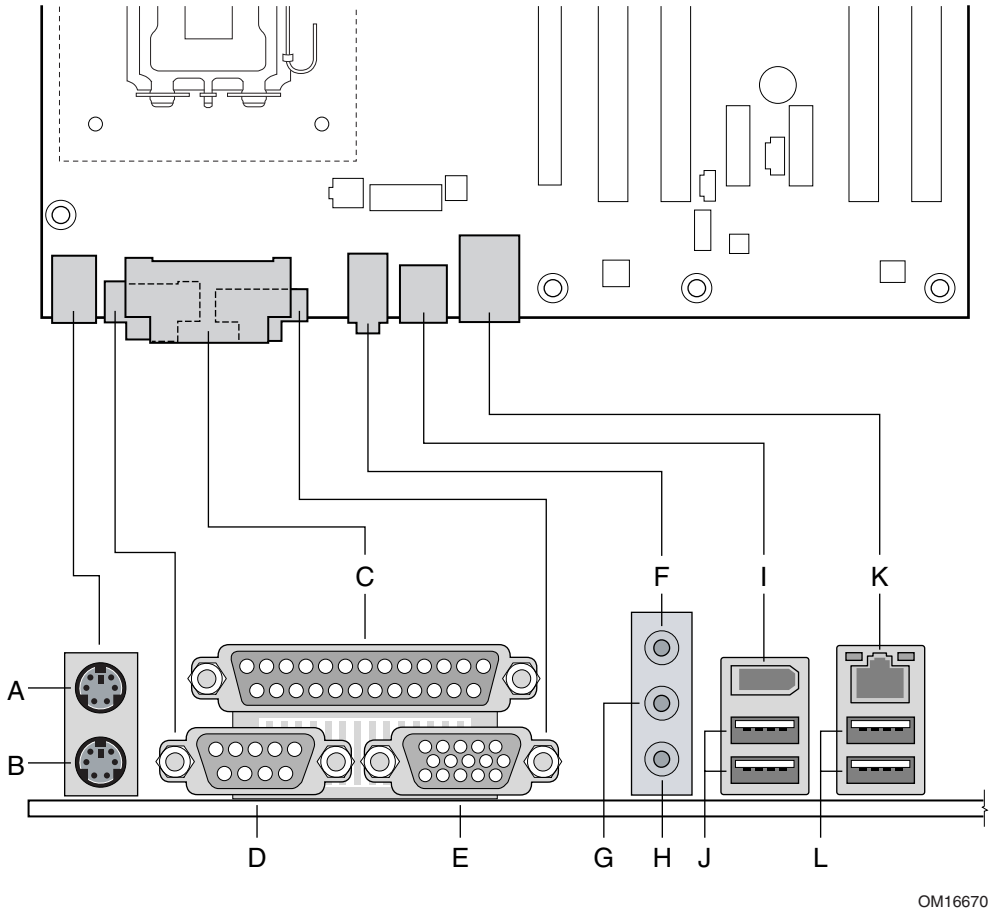


Figure 17. Back Panel Connectors

Table 18 lists the back panel connectors identified in Figure 17.

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

Table 18. Back Panel Connectors Shown in Figure 17.

Item/callout from Figure 17	Description
A	PS/2 mouse port (Green)
B	PS/2 keyboard port (Purple)
C	Parallel port (Burgundy)
D	Serial port A (Teal)
E	VGA port
F	Audio line in/Retasking Port C (Light blue)
G	Audio line out/Retasking Port D (Lime Green)
H	Mic in/Retasking Port B (Pink)
I	IEEE-1394a (optional)
J	USB ports (two)
K	LAN
L	USB ports (two)

2.8.2 Component-side Connectors

Figure 18 shows the locations of the component-side connectors on the D915GAV board.

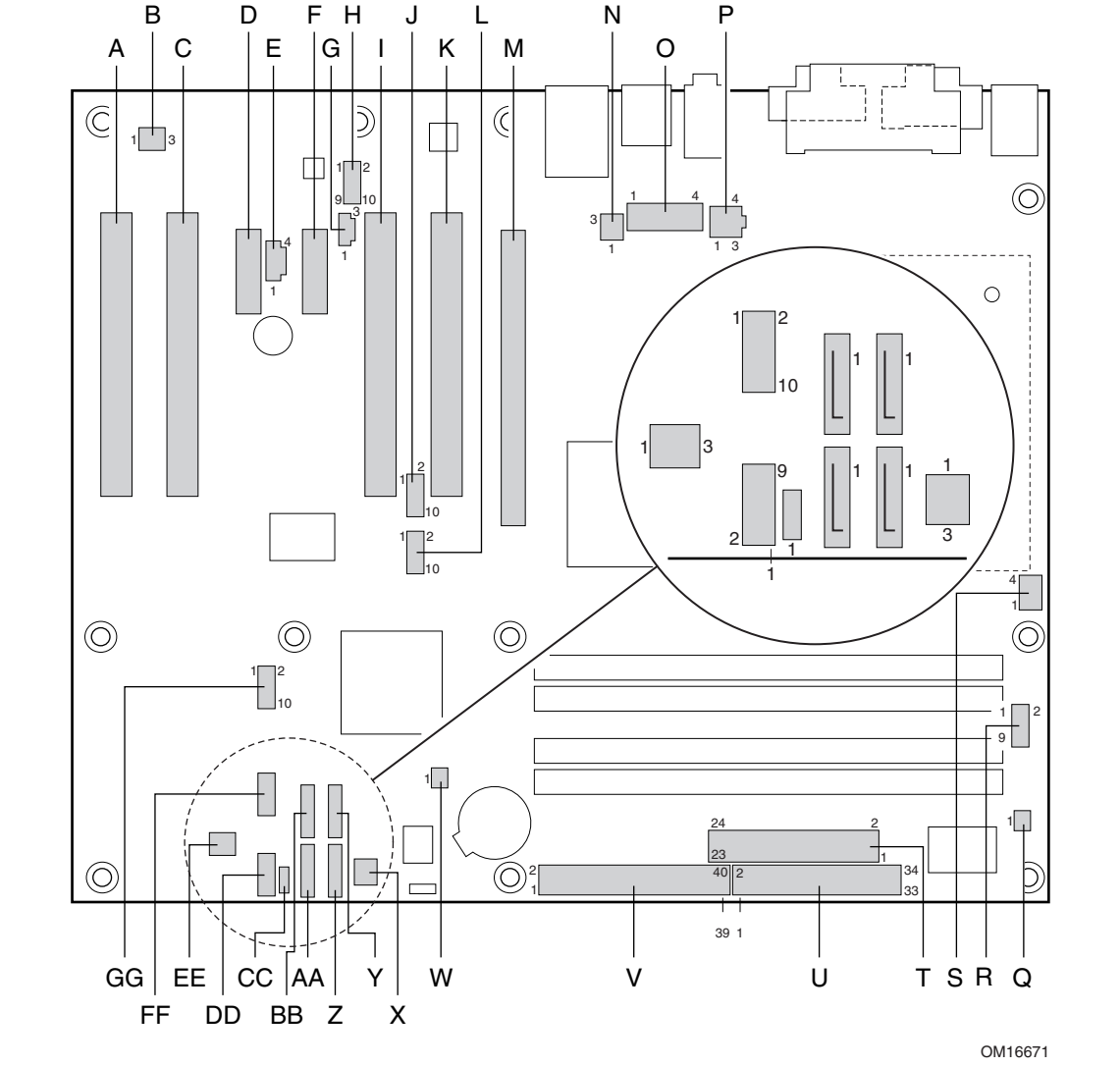


Figure 18. D915GAV Board Component-side Connectors

Table 19 lists the component-side connectors identified in Figure 18.

Table 19. Component-side Connectors Shown in Figure 18.

Item/callout from Figure 18	Description
A	PCI Conventional bus add-in card connector 4
B	Rear chassis fan connector 2
C	PCI Conventional bus add-in card connector 3
D	PCI Express x1 bus add-in card connector 2
E	ATAPI CD-ROM connector (optional)
F	PCI Express x1 bus add-in card connector 1
G	S/PDIF connector (optional)
H	Front panel audio connector
I	PCI Conventional bus add-in card connector 2
J	Front panel IEEE-1394a connector (optional)
K	PCI Conventional bus add-in card connector 1
L	Front panel IEEE-1394a connector (optional)
M	PCI Express x16 bus add-in card connector
N	Rear chassis fan connector 1
O	Alternate power connector
P	+12V power connector (ATX12V)
Q	SCSI LED (optional)
R	Serial port B (optional)
S	Processor fan connector
T	Power connector
U	Diskette drive connector
V	Parallel ATA IDE connector
W	Chassis intrusion connector
X	Front chassis fan connector
Y	Serial ATA connector 1
Z	Serial ATA connector 3
AA	Serial ATA connector 2
BB	Serial ATA connector 0
CC	Auxiliary front panel power LED connector
DD	Front panel connector
EE	ATX fan connector (optional)
FF	Front panel USB connector
GG	Front panel USB connector

Figure 19 shows the locations of the component-side connectors on the D915GAG board.

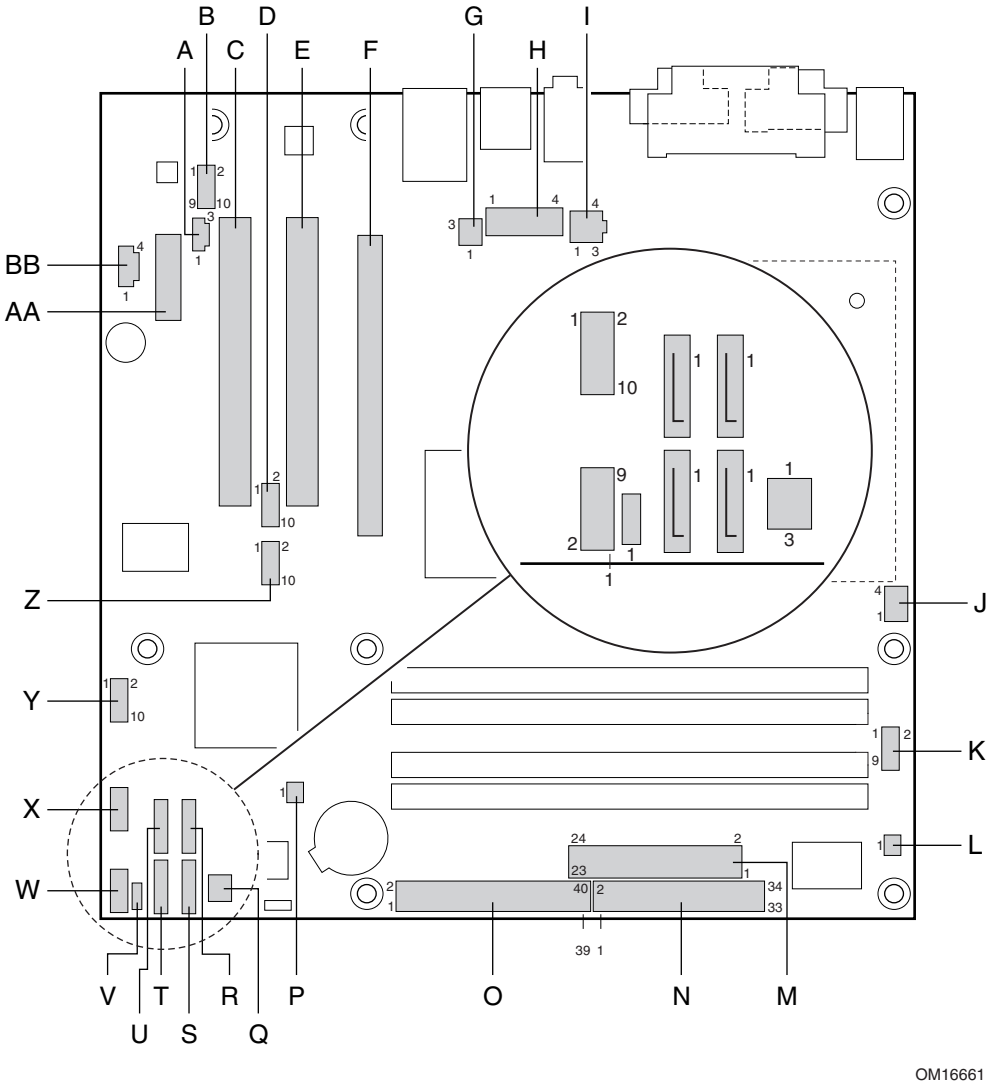


Figure 19. D915GAG Board Component-side Connectors

Table 20 lists the component-side connectors identified in Figure 19.

Table 20. Component-side Connectors Shown in Figure 19.

Item/callout from Figure 19	Description
A	S/PDIF connector (optional)
B	Front panel audio connector
C	PCI Conventional bus add-in card connector 2
D	Front panel IEEE-1394a connector (optional)
E	PCI Conventional bus add-in card connector 1
F	PCI Express x16 bus add-in card connector
G	Rear chassis fan connector
H	Alternate power connector
I	+12V power connector (ATX12V)
J	Processor fan connector
K	Serial port B (optional)
L	SCSI LED (optional)
M	Power connector
N	Diskette drive connector
O	Parallel ATA IDE connector
P	Chassis intrusion connector
Q	Front chassis fan connector
R	Serial ATA connector 1
S	Serial ATA connector 3
T	Serial ATA connector 2
U	Serial ATA connector 0
V	Auxiliary front panel power LED connector
W	Front panel connector
X	Front panel USB connector
Y	Front panel USB connector
Z	Front panel IEEE-1394a connector (optional)
AA	PCI Express x1 bus add-in card connector 1
BB	ATAPI CD-ROM connector (optional)

Table 21. S/PDIF Connector (Optional)

Pin	Signal Name
1	+5 V
2	S/PDIF Output
3	Ground

Table 22. ATAPI CD-ROM Connector (Optional)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 23. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	Port E [Port 1] Left Channel	2	Ground
3	Port E [Port 1] Right Channel	4	Presence# (dongle present)
5	Port F [Port 2] Right Channel	6	Port E [Port 1] Sense return (jack detection)
7	Port E [Port 1] and Port F [Port 2] Sense send (jack detection)	8	Key
9	Port F [Port 2] Left Channel	10	Port F [Port 2] Sense return (jack detection)

INTEGRATOR'S NOTE

The front panel audio connector is colored yellow.

Table 24. Serial Port B Connector (optional)

Pin	Signal Name	Pin	Signal Name
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	Not connected

Table 25. Chassis Intrusion Connector

Pin	Signal Name
1	Intruder
2	Ground

Table 26. SCSI Hard Drive Activity LED Connector (Optional)

Pin	Signal Name
1	SCSI_ACT#
2	No connect

Table 27. Serial ATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Table 28. Processor Fan Connector

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

2.8.2.1 Chassis Fan Connectors

The D915GAV board has three standard and one optional chassis fan connectors:

- Front chassis fan
- Rear chassis fan 1
- Rear chassis fan 2
- ATX fan connector (optional)

The D915GAG board has two chassis fan connectors:

- Front chassis fan
- Rear chassis fan

Table 29 lists the signal names for the chassis fan connectors. These signal names apply to all chassis fan connectors for both boards.

Table 29. Chassis Fan Connectors

Pin	Signal Name
1	Control
2	+12 V
3	Tach

2.8.2.2 Power Supply Connectors

The board has three power supply connectors:

- **Main power** – a 2 x 12 connector. This connector is compatible with 2 x 10 connectors previously used on Intel Desktop boards. The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables. When using a power supply with a 2 x 10 main power cable, attach that cable on the rightmost pins of the main power connector, leaving pins 11, 12, 23, and 24 unconnected.
- **ATX12V power** – a 2 x 2 connector. This connector provides power directly to the processor voltage regulator and must always be used. Failure to do so will prevent the board from booting.
- **Alternate power** – a 1 x 4 connector. This connector provides additional power when using high wattage PCI Express x16 graphics cards.

INTEGRATOR'S NOTE

When using high wattage PCI Express x16 graphics cards, use one of the following power supply configurations to avoid system instability:

- *The preferred method of power delivery is to use a power supply with a 2 x 12 main power cable. In this configuration, use two connectors to provide power to the board:*
  - *The main power connector*
  - *The ATX12V connector*

  In this configuration, the alternate power connector is not required. The 2 x 12 main power cable can provide up to 144 W of power from the +12 V rail. .
- *An alternate method of power delivery is to use a power supply has a 2 x 10 main power cable. In this configuration, use three connectors to provide power to the board:*
  - *The main power connector*
  - *The ATX12V connector*
  - *The alternate power connector*

Table 30. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V (Note)	23	+5 V (Note)
12	2 x 12 connector detect (Note)	24	Ground (Note)

Note: When using a 2 x 10 power supply cable, this pin will be unconnected.

Table 31. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 32. Alternate Power Connector

Pin	Signal Name
1	+12 V
2	Ground
3	Ground
4	+5 V

2.8.2.3 Add-in Card Connectors

The board has the following add-in card connectors:

- PCI Express x16: one connector supporting simultaneous transfer speeds up to 8 GBytes/sec.
- PCI Express x1: the D915GAV board has two PCI Express x1 connectors; the D915GAG board has one PCI Express x1 connector. The x1 interfaces support simultaneous transfer speeds up to 500 MBytes/sec.
- PCI Conventional (rev 2.2 compliant) bus: the D915GAV board has four PCI Conventional bus add-in card connectors; the D915GAG board has two PCI Conventional add-in card connectors. The SMBus is routed to PCI Conventional bus connector 2 only (ATX expansion slot 6). PCI Conventional bus add-in cards with SMBus support can access sensor data and other information residing on the Desktop Board.

Note the following considerations for the PCI Conventional bus connectors:

- All of the PCI Conventional bus connectors are bus master capable.
- SMBus signals are routed to PCI Conventional bus connector 2. This enables PCI Conventional bus add-in boards with SMBus support to access sensor data on the boards. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

NOTE

The PCI Express x16 connector is configured to support only a PCI Express x1 link when the Intel GMA900 graphics controller is enabled.

2.8.2.4 Auxiliary Front Panel Power/Sleep LED Connector

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector.

Table 33. Auxiliary Front Panel Power/Sleep LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.2.5 Front Panel Connector

This section describes the functions of the front panel connector. Table 34 lists the signal names of the front panel connector. Figure 20 is a connection diagram for the front panel connector.

Table 34. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED [Yellow]				**Power LED [Green]**			
1	HD_PWR	Out	Hard disk LED pull-up (750 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch [Purple]				**On/Off Switch [Red]**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected

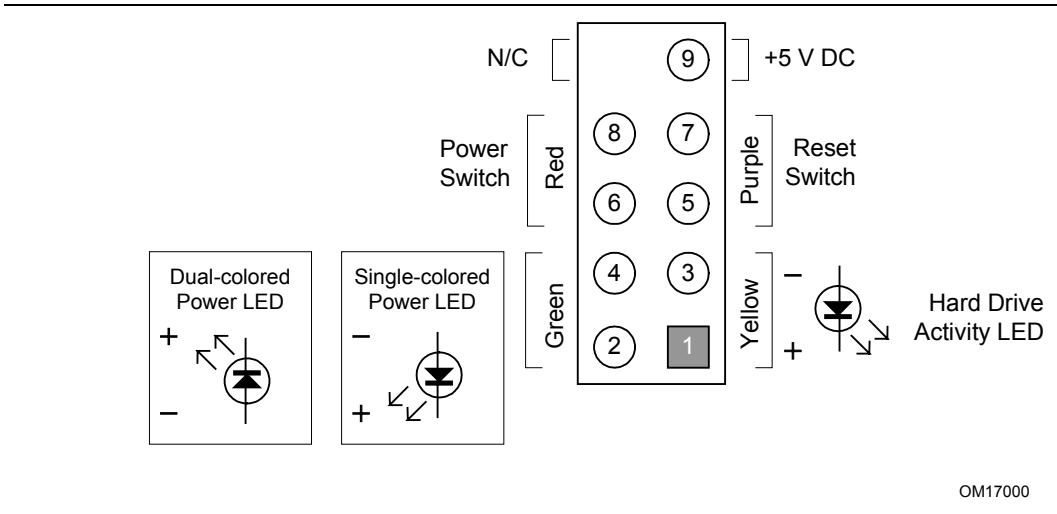


Figure 20. Connection Diagram for Front Panel Connector

2.8.2.5.1 Hard Drive Activity LED Connector [Yellow]

Pins 1 and 3 [Yellow] can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires one of the following:

- A Serial ATA hard drive connected to an onboard Serial ATA connector
- An IDE hard drive connected to an onboard IDE connector

2.8.2.5.2 Reset Switch Connector [Purple]

Pins 5 and 7 [Purple] can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.8.2.5.3 Power/Sleep LED Connector [Green]

Pins 2 and 4 [Green] can be connected to a one- or two-color LED. Table 35 shows the possible states for a one-color LED. Table 36 shows the possible states for a two-color LED.

Table 35. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 36. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

NOTE

The colors listed in Table 35 and Table 36 are suggested colors only. Actual LED colors are product- or customer-specific.

2.8.2.5.4 Power Switch Connector [Red]

Pins 6 and 8 [Red] can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.2.6 Front Panel USB Connectors

Figure 21 is a connection diagram for the front panel USB connectors.

INTEGRATOR'S NOTES

- *The +5 V DC power on the USB connector is fused.*
- *Pins 1, 3, 5, and 7 comprise one USB port.*
- *Pins 2, 4, 6, and 8 comprise one USB port.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

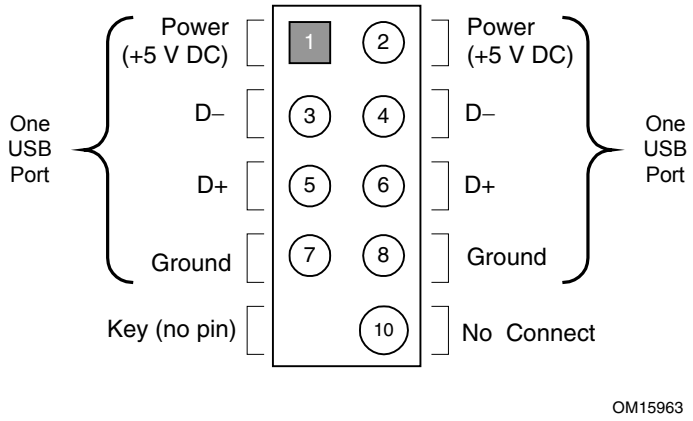


Figure 21. Connection Diagram for Front Panel USB Connectors

2.8.2.7 Front Panel IEEE 1394a Connectors (Optional)

Figure 22 is a connection diagram for the optional IEEE 1394a connectors.

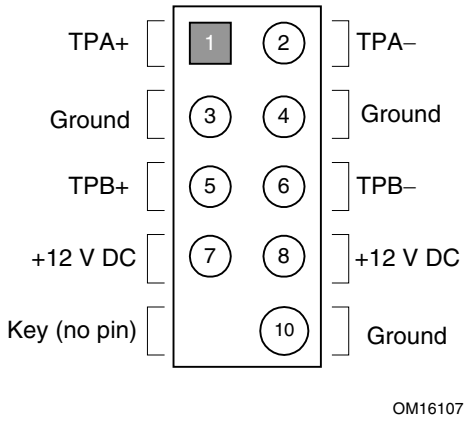


Figure 22. Connection Diagram for IEEE 1394a Connectors

INTEGRATOR'S NOTES

- *The IEEE 1394a connectors are colored blue.*
- *The +12 V DC power on the IEEE 1394a connectors is fused.*
- *Each IEEE 1394a connector provides one IEEE 1394a port.*

2.9 Jumper Block

⚠ CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 23 shows the location of the jumper block on the D915GAV board. (The jumper is in the same location on the D915GAG board.) The jumper block determines the BIOS Setup program's mode. Table 37 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

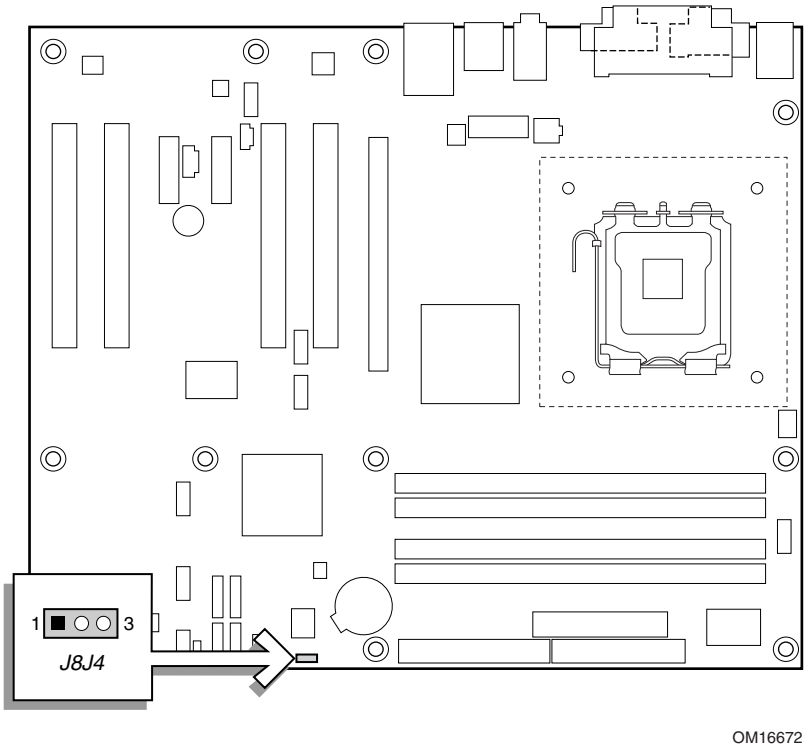


Figure 23. Location of the Jumper Block

Table 37. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2	1 3	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	1 3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None	1 3	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

2.10 Mechanical Considerations

2.10.1 D915GAV Board Form Factor

The D915GAV board is designed to fit into an ATX-form-factor chassis. Figure 24 illustrates the mechanical form factor of the board. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

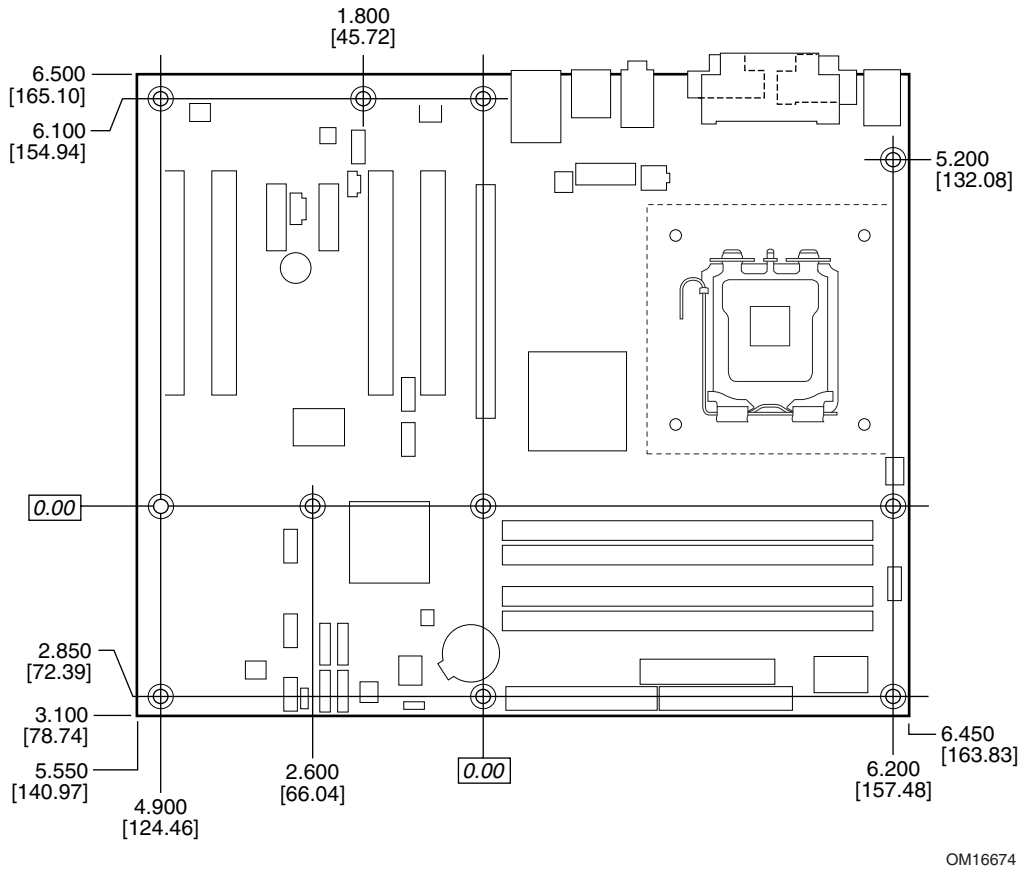


Figure 24. D915GAV Board Dimensions

2.10.2 D915GAG Board Form Factor

The D915GAG board is designed to fit into either a microATX or an ATX-form-factor chassis. Figure 25 illustrates the mechanical form factor of the board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

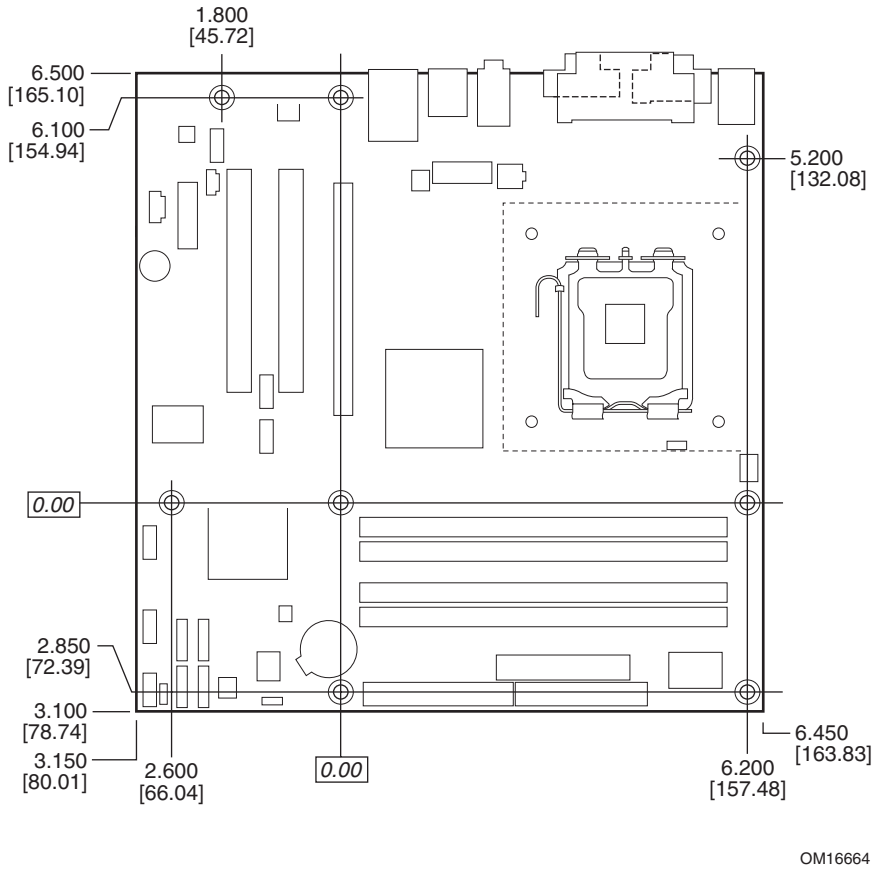


Figure 25. D915GAG Board Dimensions

2.10.3 I/O Shield

The back panel I/O shield for the boards must meet specific dimension and material requirements. Systems based on these boards need the back panel I/O shield to pass certification testing. Figure 26 shows the I/O shield. Dimensions are given in inches to a tolerance of ±0.02 inches.

The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification.

NOTE

The I/O shield drawing in this document is for reference only. An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.

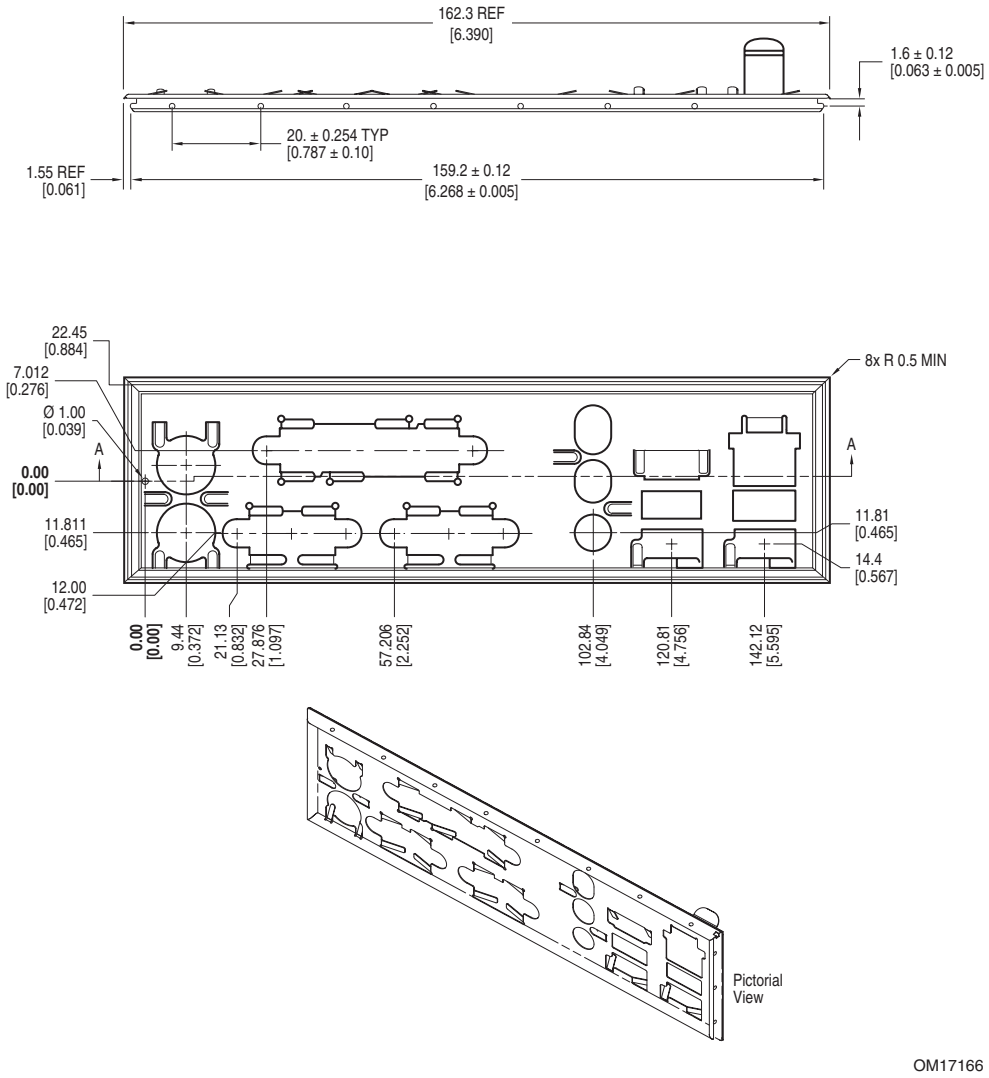


Figure 26. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 DC Loading

Table 38 lists the DC loading characteristics of the boards. This data is based on a DC analysis of all active components within the board that impact its power delivery subsystems. The analysis does not include PCI add-in cards. Minimum values assume a light load placed on the board that is similar to an environment with no applications running and no USB current draw. Maximum values assume a load placed on the board that is similar to a heavy gaming environment with a 500 mA current draw per USB port. These calculations are not based on specific processor values or memory configurations but are based on the minimum and maximum current draw possible from the board's power delivery subsystems to the processor, memory, and USB ports.

Use the datasheets for add-in cards, such as PCI, to determine the overall system power requirements. The selection of a power supply at the system level is dependent on the system's usage model and not necessarily tied to a particular processor speed.

Table 38. DC Loading Characteristics

		DC Current at:				
Mode	**DC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Minimum loading	200.00 W	3.30 A	10.00 A	900 A	0.03 A	0.80 A
Maximum loading	300.00 W	6.00 A	14.00 A	16.00 A	0.10 A	1.40 A

2.11.2 Add-in Board Considerations

The boards are designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for both boards is as follows:

- A fully loaded D915GAV board (all six expansion slots and the PCI Express x16 slot filled) must not exceed 14 A.
- A fully loaded D915GAG board (all three expansion slots and the PCI Express x16 slot filled) must not exceed 8 A.

2.11.3 Fan Connector Current Capability

CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Table 39 lists the current capability of the fan connectors.

Table 39. Fan Connector Current Capability

Fan Connector	Maximum Available Current
Processor fan	1000 mA
Front chassis fan	600 mA
Rear chassis fan	600 mA
Rear chassis fan 2	600 mA

NOTE

The rear chassis fan 2 is available only on the D915GAV board. It is not available on the D915GAG board.

2.11.4 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

System integrators should refer to the power usage values listed in Table 38 when selecting a power supply for use with the board.

Additional power required will depend on configurations chosen by the integrator.

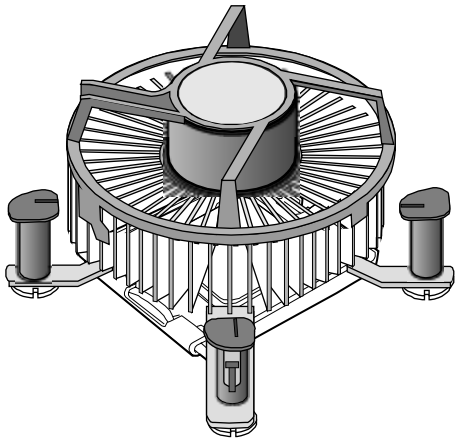
The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

2.12 Thermal Considerations

CAUTION

A chassis with a maximum internal ambient temperature of 38 °C at the processor fan inlet is a requirement. Use a processor heatsink that provides omni-directional airflow (as shown in Figure 27) to maintain required airflow across the processor voltage regulator area.



OM16996

Figure 27. Processor Heatsink for Omni-directional Airflow

CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://developer.intel.com/design/motherbd/cooling.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

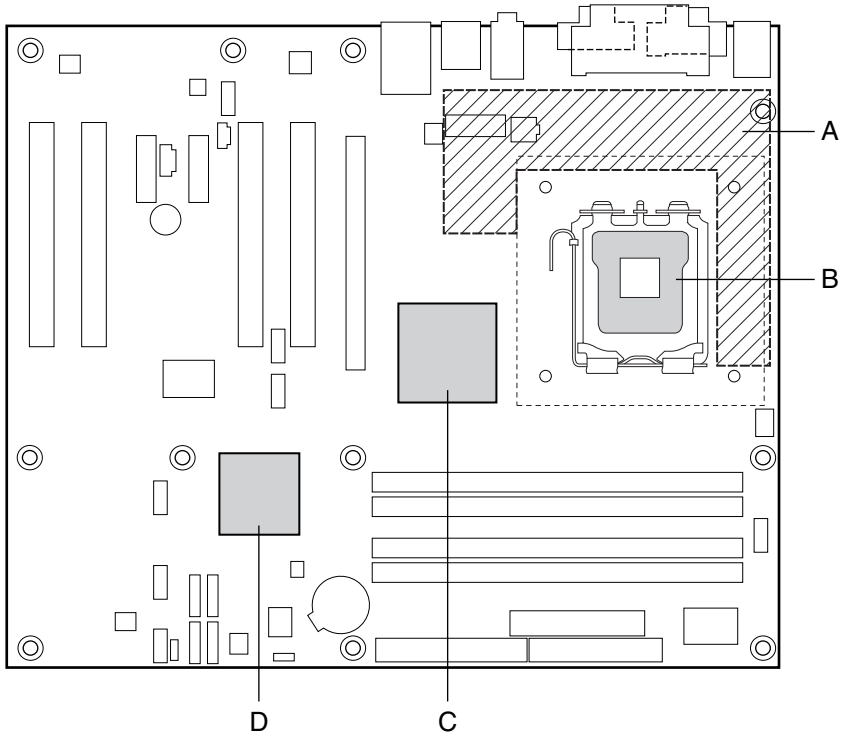
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

⚠ CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 28) can reach a temperature of up to 85 °C in an open chassis.

Figure 28 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel 82915G GMCH
D	Intel 82801FB ICH6

Figure 28. Localized High Temperature Zones

Table 40 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 40. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82915G GMCH	99 °C (under bias)
Intel 82801FB ICH6	110 °C (under bias)

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.4, page 19

2.13 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The MTBF for the D915GAV and D915GAG boards is 102,038 hours.

2.14 Environmental

Table 41 lists the environmental specifications for the board.

Table 41. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	5 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the Desktop Boards' compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 42 lists the safety regulations the Desktop Boards D915GAV and D915GAG comply with when correctly installed in a compatible host system.

Table 42. Safety Regulations

Regulation	Title
UL 60950-1:2003/ CSA C22.2 No. 60950-1-03	Information Technology Equipment - Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1:2002	Information Technology Equipment - Safety - Part 1: General Requirements (European Union)
IEC 60950-1:2001, First Edition	Information Technology Equipment - Safety - Part 1: General Requirements (International)

2.15.2 EMC Regulations

Table 43 lists the EMC regulations the Desktop Boards D915GAV and D915GAG comply with when correctly installed in a compatible host system.

Table 43. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)
VCCI (Class B)	Voluntary Control for Interference by Information Technology Equipment (Japan)

2.15.2.1 FCC Compliance Statement (USA)

Product Type: D915GAV Desktop Board and D915GAG Desktop Board

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to a different electrical branch circuit from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

2.15.2.2 Canadian Compliance Statement

This Class B digital apparatus complies with Canadian ICES-003.

Cet appereil numérique de la classe B est conforme à la norme NMB-003 du Canada.

2.15.3 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product: Intel® Desktop Boards D915GAV and D915GAG are in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 89/336/EEC & 73/23/EEC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 89/336/EEC & 73/23/EEC.

Suomi Tämä tuote noudattaa EU-direktiivin 89/336/EEC & 73/23/EEC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 89/336/EEC & 73/23/EEC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 89/336/EEC & 73/23/EEC.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 89/336/ EEC & 73/23/EEC.

Italiano Questo prodotto è conforme alla Direttiva Europea 89/336/EEC & 73/23/EEC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 89/336/ EEC & 73/23/EEC.

Portuguese Este produto cumpre com as normas da Diretiva Européia 89/336/EEC & 73/23/EEC.

Español Este producto cumple con las normas del Directivo Europeo 89/336/EEC & 73/23/EEC.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 89/336/EEC & 73/23/EEC.

2.15.4 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

2.15.4.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

2.15.4.2 Recycling Considerations

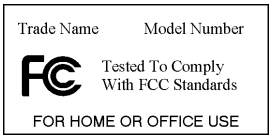
Intel encourages its customers to recycle its products and their components (e.g., batteries, circuit boards, plastic enclosures, etc.) whenever possible. In the U.S., a list of recyclers in your area can be found at:
http://www.eiae.org/

In the absence of a viable recycling option, products and their components must be disposed of in accordance with all applicable local environmental regulations.

2.15.5 Product Certification Markings (Board Level)

Table 44 lists the board's product certification markings.

Table 44. Product Certification Markings

Description	Marking
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882 (component side).	
FCC Declaration of Conformity logo mark for Class B equipment; includes Intel name and D915GAV or D915GAG model designation (component side).	
CE mark. Declares compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.	
Australian Communications Authority (ACA) C-Tick mark. Includes adjacent Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.	
Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0 or 94V-0

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction 89
3.2 BIOS Flash Memory Organization 90
3.3 Resource Configuration 90
3.4 System Management BIOS (SMBIOS) 91
3.5 Legacy USB Support 91
3.6 BIOS Updates 92
3.7 Boot Options 93
3.8 Fast Booting Systems with Intel® Rapid BIOS Boot 94
3.9 BIOS Security Features 95

3.1 Introduction

The boards use an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as EV91510A.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the Desktop Board is in configure mode. Section 2.9 on page 75 shows how to put the Desktop Board in configure mode.

Table 45 lists the BIOS Setup program menu features.

Table 45. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 46 lists the function keys available for menu screens.

Table 46. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 BIOS Flash Memory Organization

The Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the PCI IDE connector with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and

to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.

5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.4, page 19

3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Additional languages are available in the Integrator's Toolkit utility. Check the Intel website for details.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

✏ NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
The Intel World Wide Web site	Section 1.4, page 19

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 47 lists the boot device menu options.

Table 47. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.8 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS

3.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.8.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enable Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 48 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 48. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Error Messages and Beep Codes

What This Chapter Contains

4.1 BIOS Error Messages 97
4.2 Port 80h POST Codes 99
4.3 Bus Initialization Checkpoints 103
4.4 Speaker 104
4.5 BIOS Beep Codes 104

4.1 BIOS Error Messages

Table 49 lists the error messages and provides a brief description of each.

Table 49. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.
Checking NVRAM.....	NVRAM is being checked to see if it is valid.

continued

Table 49. BIOS Error Messages (continued)

Error Message	Explanation
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM/CMOS/PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

4.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

✏ NOTE

The POST card must be installed in PCI bus connector 1.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 50 defines the uncompressed INIT code checkpoints, Table 51 describes the boot block recovery code checkpoints, and Table 52 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 50. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 51. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 52. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 4.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 4.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 4.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 52. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 52. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 4.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 52. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

4.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 53 describes the bus initialization checkpoints.

Table 53. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 54 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 54. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 55 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 55. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

4.4 Speaker

A 47 Ω inductive speaker is mounted on the board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, on page 14

4.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 56). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters). If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 56. Beep Codes

Beep	Description
1	CPU error
3	Memory error
6	System failure
7	System failure
8	Video error